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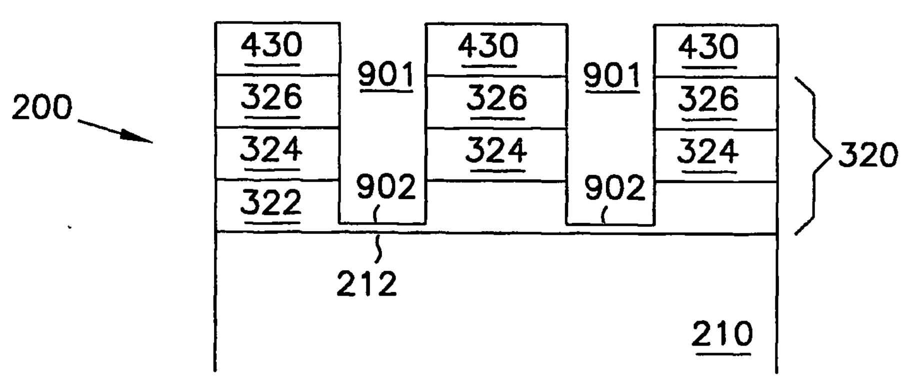
(54) **Title:** TRANSPARENT AMORPHOUS CARBON STRUCTURE IN SEMICONDUCTOR DEVICES



(57) **Abstract:** A transparent amorphous carbon layer is formed. The transparent amorphous carbon layer has a low absorption coefficient such that the amorphous carbon is transparent in visible light. The transparent amorphous carbon layer may be used in semiconductor devices for different purposes. The transparent amorphous carbon layer may be included in a final structure in semiconductor devices. The transparent amorphous carbon layer may also be used as a mask in an etching process during fabrication of semiconductor devices.

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TRANSPARENT AMORPHOUS CARBON STRUCTURE IN SEMICONDUCTOR DEVICES

Related Applications

This application is related to the following co-pending and commonly assigned application; attorney docket number 303.869US1, application serial number 10/661,100 entitled "MASKING STRUCTURE HAVING MULTIPLE LAYERS INCLUDING AN AMORPHOUS CARBON LAYER" which is hereby incorporated by reference.

Field of Invention

The present invention relates generally to semiconductor devices, more particularly to masking structures in the semiconductor devices.

Background

Semiconductor devices such as memory devices reside in many computers and electronic products to store data. A typical semiconductor device has many layers of different materials formed on a semiconductor wafer.

During manufacturing, the layers go through many processes. For example, a patterning process puts patterns on the layers. Some patterning processes use a mask to transfer patterns from the mask to the layers underneath the mask.

Some conventional masks are made of amorphous carbon. However, an amorphous carbon mask at some thickness may have a high absorption of optical light, causing the amorphous carbon mask inapplicable for some processes.

Summary of the Invention

The present invention provides devices having a masking structure and techniques for forming the masking structure. The masking structure includes an amorphous carbon layer having a low absorption property. The amorphous layer is transparent in visible light range of the electromagnetic radiation.

Brief Description of the Drawings

FIG. 1A is a flow chart showing a method of forming an amorphous carbon layer according an embodiment of the invention.

FIG. 1B is graph showing an absorption coefficient (k) at an exemplary wavelength versus deposition temperature of a transparent amorphous carbon layer according to an embodiment of the invention.

FIG. 1C is graph showing an absorption coefficient (k) at exemplary temperatures versus range of wavelengths of a transparent amorphous carbon according to an embodiment of the invention.

FIG. 1D is graph showing a transmission percentage versus a range of wavelengths of several transparent amorphous carbon layers at exemplary temperatures and exemplary thicknesses according to an embodiment of the invention.

FIG. 1E is graph showing an exemplary deposition rate versus a temperature range of a method of forming a transparent amorphous carbon layer according to an embodiment of the invention.

FIG. 2 through FIG. 10 show cross-sections of a device during various processing stages according to embodiments of the invention.

FIG. 11 through FIG. 19 show cross-sections of a memory device during various processing stages according to embodiments of the invention.

FIG. 20 shows a system according to an embodiment of the invention.

Detailed Description of the Embodiments

The following description and the drawings illustrate specific embodiments of the invention sufficiently to enable those skilled in the art to practice the invention. Other embodiments may incorporate structural, logical, electrical, process, and other changes. In the drawings, like numerals describe substantially similar components throughout the several views. Examples merely typify possible variations. Portions and features of some embodiments may be included in or substituted for those of others. The scope of the invention encompasses the full ambit of the claims and all available equivalents.

FIG. 1A is flowchart showing a method of forming an amorphous carbon layer according to an embodiment of the invention. Method 100 forms an

amorphous carbon layer having a low absorption coefficient such that the amorphous carbon layer is transparent in visible light range.

The visible light range is the range (optical range) of the electromagnetic spectrum having light (electromagnetic radiation) visible to human eyes. The visible light range includes any light having a wavelength between about 400 nm (nanometers) and about 700 nm. The non-visible light range is the range of the entire electromagnetic spectrum minus the visible light range. Some examples of the non-visible light range include electromagnetic radiations with wavelengths between 700 nm and one millimeter (infrared light), wavelengths between 10 nm and 400 nm (ultraviolet light), and wavelengths between .01 nm and 10 nm (X-ray).

In this specification, the amorphous carbon layer is transparent in visible light range means that the amorphous carbon layer has a substantially low absorption coefficient (*k*) in which *k* has a range between about 0.15 and about 0.001 at wavelength of 633 nm. In some embodiments, the amorphous carbon layer transparent in visible light range is an amorphous carbon layer formed at a temperature from about 200°C to about 500°C such that the amorphous carbon layer has an absorption coefficient (*k*) between about 0.15 and about 0.001 at wavelength of 633 nm.

At box 102 of method 100 in FIG. 1A, a wafer is placed in a chamber. In some embodiments, the chamber is a chemical vapor deposition chamber and the wafer is a semiconductor wafer. In embodiments represented by FIG. 1A, the chamber is a plasma enhanced chemical vapor deposition (PECVD) chamber.

At box 104, the parameters are set for the process of forming an amorphous carbon layer according to the invention. The parameters include temperature, gas mixture, gas flow rate, power, and pressure. The temperature in the chamber is set to a selected temperature. The selected temperature is any temperature from about 200°C to about 500°C. In some embodiments, the temperature is set between about 200° C and below 300° C. In other embodiments, the temperature is set between about 225° C and about 375° C.

In the process of forming an amorphous carbon layer, a process gas including propylene (C_3H_6) is introduced into the chamber at a flow rate. In some embodiments, the flow rate of the propylene is set between about 500

standard cubic centimeters per minute (sccm) and about 3000 sccm. An additional gas including helium may be also introduced into the chamber at a flow rate. In some embodiments, the flow rate of the helium is set between about 250 sccm and about 1000 sccm. Further, embodiments exist where at least one of the other hydrocarbon gases is used as the process gas. Examples of the other hydrocarbon gases include CH_4, C_2H_2, C_2H_4, C_2H_6, and C_3H_8. Helium may also be used in combination with at least one of these hydrocarbon gases. Thus, in box 104, a gas mixture is introduced into the chamber.

In this specification, the gas mixture may be either one gas only or a combination of at least two gases. For example, the gas mixture may be either propylene (C_3H_6) only or a combination of propylene and helium. As another example, the gas mixture may be at least one of the propylene, CH_4, C_2H_2, C_2H_4, C_2H_6, and C_3H_8. As a further example, the gas mixture may be at least one of the propylene, CH_4, C_2H_2, C_2H_4, C_2H_6, and C_3H_8 plus helium.

During the process of forming the amorphous carbon layer in method 100, the chamber is subjected to a radio frequency (RF) power and a pressure. In some embodiments, the radio frequency power is set between about 450 Watts and about 1000 Watts, and the pressure is set between about 4 Torr and about 6.5 Torr.

In box 106, an amorphous carbon layer is formed as a deposited layer over the wafer. The amorphous carbon layer is transparent in visible light range. In some embodiments, the amorphous carbon layer formed by method 100 has an absorption coefficient (k) between about 0.15 and about 0.001 at wavelength of 633 nm.

Since the amorphous carbon layer formed by method 100 is transparent in visible light range, the amorphous carbon layer formed by method 100 is also referred to as a transparent amorphous carbon layer. Thus, the transparent amorphous carbon layer refers to an amorphous carbon layer formed according method 100 in which the temperature is set from about 200°C to about 500°C.

The transparency of the amorphous carbon layer formed by method 100 depends in part on the temperature set during the process. In method 100, the transparency of the amorphous carbon layer formed to a specific thickness at a lower temperature is more transparent than the amorphous carbon layer formed

to that specific thickness at a higher temperature. For example, in method 100, the amorphous carbon layer formed to a thickness at 200°C is more transparent than the amorphous carbon layer formed to the same thickness at 500°C.

The transparent amorphous carbon layer formed by method 100 may be used in semiconductor devices such as memory devices and microprocessors. For example, the transparent amorphous carbon layer formed by method 100 may be included in a structure of semiconductor devices as an insulating layer or an antireflective layer. As another example, the transparent amorphous carbon layer formed by method 100 may also be used as a mask in an etching process during manufacturing of semiconductor devices.

FIG. 1B is graph showing absorption coefficient (k) at an exemplary wavelength versus deposition temperature of a transparent amorphous carbon layer according to an embodiment of the invention. In some embodiments, the graph of FIG. 1B shows the absorption coefficient of the transparent amorphous carbon layer formed according to the method described in FIG. 1A.

In FIG. 1B, curve 150 shows the transparent amorphous layer having an absorption coefficient k ranging from about 0.15 to about 0.001 at wavelength of 633 nm when the transparent amorphous layer is formed (or deposited) at a temperature from about 200°C to about 500°C. In FIG. 1B, curve 150 has an exemplary shape. In some embodiments, curve 150 may have a shape different from the shape shown in FIG. 1B.

FIG. 1C is graph showing absorption coefficient (k) at exemplary temperatures versus a range of wavelengths of a transparent amorphous carbon according to an embodiment of the invention. In some embodiments, the graph of FIG. 1C shows the absorption coefficient of the transparent amorphous carbon layer formed according to the method described in FIG. 1A.

In FIG. 1C, curve 161 shows absorption coefficient (k) versus a range of wavelengths of a transparent amorphous carbon formed at an exemplary temperature of 375°C. Curve 162 shows absorption coefficient versus a range of wavelengths of another transparent amorphous carbon formed at an exemplary temperature of 225°C.

FIG. 1D is graph showing transmission percentage versus a range of wavelengths of several transparent amorphous carbon layers at exemplary

temperatures and exemplary thicknesses according to an embodiment of the invention. In some embodiments, the graph of FIG. 1D shows exemplary transmission percentages of the transparent amorphous carbon layer formed according to the method described in FIG. 1A.

In FIG. 1D, curves 171, 172, and 173 show transmission percentage versus a range of wavelengths for three different amorphous carbon layers formed to different thickriesses at different temperatures. Curve 171 shows transmission percentage versus a range of wavelengths of a transparent amorphous carbon layer formed to a thickness of 3000 Angstroms at a temperature of 225°C. Curve 172 shows transmission percentage versus the range of wavelengths of a transparent amorphous carbon layer formed to a thickness of 3000 Angstroms at a temperature of 375°C. Curve 173 shows transmission percentage versus the range of wavelengths of a transparent amorphous carbon layer formed to a thickness of 7000 Angstroms at a temperature of 375°C. FIG. 1D shows that the transmission increases when the thicknesses, or the temperature, or both decreases.

FIG. 1E is graph showing exemplary deposition rate versus a temperature range of a method of forming a transparent amorphous carbon layer according to an embodiment of the invention. In some embodiments, the graph of FIG. 1E shows exemplary deposition rate of the transparent amorphous carbon layer formed according to the method described in FIG. 1A. FIG. 1E shows that the deposition rate is inversely proportional to the temperature. For example, at a temperature of 250°C, the deposition rate is about 2800 Angstroms per minute. As another example, at a temperature of 400°C, the deposition rate is about 2100 Angstroms per minute.

FIG. 2 through FIG. 10 show a device 200 during various processing stages according to embodiments of the invention.

FIG. 2 shows a cross-section of a device 200 including a substrate 210. Substrate 210 may represent a part of a wafer, or may be a wafer itself. The wafer may be a semiconductor wafer such as a silicon wafer. Substrate 210 may also be a structure or a layer formed on a wafer. Substrate 210 may include at least one of a non-conducting material, a conducting material, and a semiconducting material. Examples of non-conducting materials include oxide

(e.g., SiO_2, Al_2O_3), nitride (e.g., Si_3N_4), and glass (borophosphosilicate glass-BPSG). Examples of conducting materials include aluminum, tungsten, other metals, and compound of metals. Examples of semiconducting materials include silicon, and silicon doped with other materials such as boron, phosphorous, and arsenic. In embodiments represented by FIG. 2, substrate 210 includes a semiconductor material.

Substrate 210 has a surface 212 in which alignment marks 214 are formed. Alignment marks 214 serves as reference points or coordinates of substrate (wafer) 210. During an alignment process, the alignment marks 214 are used to align or position substrate 210 such that structures and layers on substrate 210 can be accurately aligned with each other or with substrate 210.

FIG. 3 shows device 200 with a device structure 320 formed over substrate 210. Device structure 320 includes multiple layers 322, 324, and 326. Each of these multiple layers may include at least one of a non-conducting material, semiconducting material, and a conducting material. For example, layer 322 may be an oxide layer; layer 324 may be a metal layer or a layer having a compound of metal and silicon; and layer 326 may be a nitride layer. In some embodiments, multiple layers 322, 324, and 326 are arranged in an order different from the order shown in FIG. 3. Multiple layers 322, 324, and 326 are formed by growing or deposition or by other known processes. In some embodiments, one or more of the layers 322, 324, and 326 is omitted from device structure 320. In other embodiments, one or more additional layers similar to layers 322, 324, and 326 are added to device structure 320. Device structure 320 has a thickness T3. In some embodiments, T3 is at least 40000 Angstroms.

FIG. 4A shows device 200 with a mask (layer) 430 formed over device structure 320. Mask 430 is made of carbon. In embodiments represented by FIG. 4A, the carbon is amorphous carbon. Thus, in FIG. 4A, mask 430 is also referred to as amorphous carbon layer 430. Amorphous carbon layer 430 may be formed by a method similar to method 100 described in FIG. 1A.

Amorphous carbon layer 430 has a thickness T4. T4 can be any thickness. In some embodiments, T4 is at leas 4000 Angstroms. Amorphous carbon layer 430 has a low absorption coefficient such that amorphous carbon

layer 430 is transparent in visible light range. In some embodiments, amorphous carbon layer 430 has an absorption coefficient (k) between about 0.15 and about 0.001 at wavelength of 633 nm.

Since amorphous carbon layer 430 is transparent in visible light range, amorphous carbon layer 430 does not substantially absorb or reflect the light in the visible light range. Therefore, the transparency in visible light range property of amorphous carbon layer 430 improves the reading of alignment marks 214 (FIG. 2) on substrate 210 during the alignment of substrate 210. Further, since amorphous carbon layer 430 is transparent in visible light range, the thickness of amorphous carbon layer 430 may not be limited. Thus, amorphous carbon layer 430 may be formed with a thickness to properly etch device structure 320 while allowing an accurate reading of the alignment marks such as alignment marks 214.

In comparing amorphous carbon layer 430 with a conventional amorphous carbon layer having a higher absorption coefficient (or less transparent) than that of amorphous carbon layer 430, the conventional amorphous carbon may have a thickness limitation for some processes. For example, some process may require a mask with a specific thickness, using a conventional amorphous carbon layer with the specific thickness may cause difficulty in reading the alignment marks or may result in inaccurate reading because of the high absorption property of the conventional amorphous carbon layer. Therefore, because of the low absorption property, amorphous carbon layer 430 is useful in processes that may require a mask with a specific thickness in which a conventional amorphous carbon mask is unsuitable.

Amorphous carbon layer 430 of device 200 is formed with a thickness sufficient to properly etch a device structure such as device structure 320. For example, amorphous carbon layer 430 is formed with thickness T4 equal to or greater than about 4000 Angstroms to etch device structure 320 with thickness T3 equal to or greater than 40000 Angstroms.

FIG. 4B shows device 200 with a cap layer 540 formed over amorphous carbon layer 430. In some embodiments, cap layer 540 includes oxide materials. In other embodiments, cap layer 540 includes non-oxide materials. In FIG. 4B, cap layer 540 includes silicon oxynitride ($Si_xO_yN_z$) or silicon-rich oxide (Si_xO_y)

where x, y, and z are real numbers. In some embodiments, cap layer 540 includes hydrogenated silicon oxynitride ($Si_xO_yN_z$:H) or hydrogenated silicon-rich oxide (Si_xO_y:H).

Cap layer 540 can be formed by a deposition process such as a CVD and PECVD process. In some embodiments, cap layer 540 is formed together with amorphous carbon layer 430 in the same process (same processing step) such that cap layer 540 is situ deposited over amorphous carbon layer 430.

FIG. 5 shows device 200 with a photoresist layer 550 formed over cap layer 540 and amorphous carbon layer 430. Photoresist 550 is formed using known techniques. In some embodiments, cap layer 540 serves as an antireflective layer for reducing the reflection to photoresist layer 550 from layers underneath amorphous carbon layer 430 during patterning of photoresist layer 550. Reducing the reflection allows more accurate patterning of photoresist layer 550. In other embodiments, cap layer 540 serves as a mask for patterning amorphous carbon layer 430. In some other embodiments, cap layer 540 serves as both an antireflective layer and as a mask.

The combination of amorphous carbon layer 430, cap layer 540, and photoresist layer 550 forms a masking structure 560. In some embodiments, cap layer 540 is omitted from masking structure 560. In other embodiments, besides amorphous carbon layer 430, cap layer 540, and photoresist layer 550, masking structure 560 further includes an additional layer formed between photoresist layer 550 and cap layer 540. The additional layer serves as an antireflective layer to further enhance the photo processing performance.

FIG. 6 shows device 200 after photoresist layer 550 is patterned. Patterning photoresist layer 550 can be performed using known techniques. In FIG. 6, patterned photoresist layer 550 has openings 652. Patterned photoresist layer 550 is used as a mask to pattern cap layer 540 and amorphous carbon layer 430.

FIG. 7 shows device 200 after the masking structure 560 is patterned. Patterning masking structure 560 can be performed by one or more etching steps. In some embodiments, cap layer 540 and amorphous carbon layer 430 are etched together in one etching step. In other embodiments, cap layer 540 and amorphous carbon layer 430 are etched separately in different etching steps. As

shown in FIG. 7, each of the patterned cap layer 540 and the patterned amorphous carbon layer 430 has openings that are continuous and aligned with openings 652 of photoresist layer 550. In some embodiments, after amorphous carbon layer 430 is patterned, the combination of layers 430, 540, and 550 of masking structure 560 may remain and is used as a mask to etch the layers of device structure 320. In other embodiments, after amorphous carbon layer 430 is patterned, either photoresist layer 550 or a combination of both photoresist layer 550 and cap layer 540 is removed. The remaining (not removed) layer, or layers, of masking structure 560 is used as a mask to etch one or both of device structure 320 and substrate 210.

FIG. 8 shows device 200 after both photoresist layer 550 and cap layer 540 are removed. In this example, the remaining amorphous carbon layer 430 is used as a mask to etch either a portion of device structure 320, or the entire device structure 320. In some embodiments, at least a portion of substrate 210 is also etched using amorphous carbon layer 430 as a mask

FIG. 9 shows device 200 after device structure 320 is etched. Trenches 901 are formed as a result of the etching process. In embodiments represented by FIG. 9, trenches 901 are formed in at least portion of device structure 320. In some embodiments, trenches 901 are formed in the entire device structure 320 and in at least a portion of substrate 210.

Layer 322 is etched to a level 902. Level 902 is any level above surface 212 of substrate 210. In embodiments represented by FIG. 9, device structure 320 is etched such that the etching process penetrates through layers 326 and 324 and partially into layer 324 and stopping at level 902. In some embodiments, device structure 320 is etched such that level 902 can be anywhere in device structure 320. In other embodiments, the etching process penetrates through all layers 322, 324, and 326 and stops at or below surface 212 of substrate 210. The level at which the etching process etches into device structure 320 depends on what will be formed after device structure 320 is etched. For example, device structure 320 is etched to one level if conductive interconnects will be formed and device structure 320 is etched to another level if a component such as a capacitor will be formed.

FIG. 10 shows device 100 after amorphous carbon layer 430 is removed. In some embodiments, amorphous carbon layer 430 is removed using an ash process with oxygen plasma. In other embodiments, amorphous carbon layer 430 is removed using an ash process with a combination of oxygen plasma and CF_4.

In the above description of FIG. 4A through FIG. 10, amorphous carbon layer 430, which is transparent in visible light range, is included in masking structure 560 to use as a mask to etch device structure 320. In some embodiments, an amorphous carbon layer such as amorphous carbon layer 430 is also included in device structure 320. For example, one of the layers 322, 324, and 326 of device structure 320 may be an amorphous carbon layer such as amorphous carbon layer 430. As another example, device structure 320 may include an additional layer besides layer 322, 324, and 326 in which the additional layer is an amorphous carbon layer such as amorphous carbon layer 430.

In embodiments where an amorphous carbon layer exists within device structure 320, the amorphous carbon layer within device structure 320 may be used for insulating purposes, antireflection purposes, or for other purposes. Hence, in embodiments where device structure 320 includes an amorphous carbon layer similar to amorphous carbon layer 430, the amorphous carbon layer of device structure 320 still remains in device 200 after amorphous carbon layer 430 of masking structure 560 is removed from device 200.

After amorphous carbon layer 430 is removed as shown in FIG. 10, other processes can be performed to device 200 to form components such as transistors, capacitors, memory cell, or an integrated circuit such as a memory device, a processor, an application specific integrated circuit, or other types of integrated circuits.

FIG. 11 through FIG. 19 show cross-sections of a memory device 1100 during various processing stages according to embodiments of the invention. In FIG. 11, memory device 1100 includes a substrate 1102 having alignment marks 1104 formed on surface 1107 of substrate 1102. A number of surface structures (gate structures) 1105 (1105.1 through 1105.4) are formed over substrate 1102. Within substrate 1102, a number of diffusion regions 1106 (1106.1 through

1106.3) and isolation structures 1107.1 and 1107.2 are formed. For clarity, FIG. 11 shows alignment marks 1104 without elements formed above alignment marks 1104. However, elements such as the layers shown in FIG. 11 may be formed over alignment marks 1104.

Memory device 1100 also includes an insulating layer 1130 and a number of contacts 1140 (1140.1 through 1140.3) extending through insulating layer 1130. Each of the contacts 1140 connects to one of the diffusion regions 1106. A barrier layer 1145 separates surface structures 1105 from insulating layer 1130 and contacts 1140. Contacts 1140 are made of conducting material to provide electrical connections for diffusion regions 1106. Barrier layer 1145 can be oxide, or nitrite, or other non-conducting materials to prevent cross-diffusion of materials between surface structures 1105 and insulating layer 1130. In some embodiments, barrier layer 1145 is omitted. Insulating layer 1130 provides insulation between the contacts 1140. Insulating layer 1130 can be a layer of silicate glass doped with one or more dopants such as boron and phosphorous or other types of doped glasses. For example, insulating layer 1130 can be Boronsilicate glass (BSG), or Phosphosilicate glass (PSG). In embodiments represented by FIG. 11, insulating layer 1130 includes Borophosphosilicate glass (BPSG) and has a thickness T11. In some embodiments, T11 is in the range of 3000 Angstroms to 5000 Angstroms.

In embodiments represented by FIG. 11, substrate 1102 includes silicon doped with a dopant, for example boron, to make it a P-type material. Diffusion regions 1106 are doped with a dopant, for example phosphorous, to make them an N-type material. In some embodiments, substrate 1102 can be an N-type material and diffusion regions 1106 can be a P-type material.

Each of the gate structures 1105 includes a number of elements: a gate dielectric (gate oxide) 1109, a doped polysilicon layer 1112, a silicide layer 1114, a capping dielectric layer 1116, and dielectric spacers 1118. Silicide layer 1114 can include a compound of metal and silicon such as titanium silicide, tungsten silicide, and others. All dielectrics in gate structures 1105 can include material such as silicon oxide. Each of the gate structures 1105 is also referred to as a word line. The structure of FIG. 11 can be formed using known techniques.

FIG. 12 shows memory device 1100 after an insulating layer 1210 is formed. Insulating layer 1210 can include BSG, PSG, or BPSG similar to insulating layer 1130. Insulating layer 1210 and other structures in FIG. 12 form a device structure 1220. Device structure 1220 has a thickness T12. In some embodiments, T12 is at least 40000 Angstroms.

FIG. 13 shows memory device 1100 after an amorphous carbon layer 1330 is formed over device structure 1220. Amorphous carbon layer 1330 has a low absorption coefficient such that amorphous carbon layer 1330 is transparent in visible light range. In some embodiments, amorphous carbon layer 1330 has an absorption coefficient (*k*) between about 0.15 and about 0.001 at wavelength of 633 nm. Amorphous carbon layer 1330 may be formed by a method similar to method 100 described in FIG. 1A.

Since amorphous carbon layer 430 is transparent in visible light range, amorphous carbon layer 1330 may be formed at a selected thickness to properly etch device structure 1220 without substantially affecting the reading of the alignment marks 1104 during an alignment of device 1100. Amorphous carbon layer 1330 has a thickness T13, which can be selected at an appropriate value to properly etch device structure 1220. T13 can be any thickness. In some embodiments, T13 is at least 4000 Angstroms.

FIG. 14 shows memory device 1100 after a cap layer 1440 and a photoresist layer 1450 are formed over amorphous carbon layer 1330. In some embodiments, cap layer 1440 includes oxide materials. In other embodiments, cap layer 1440 includes non-oxide materials. In FIG. 14, cap layer 1440 includes silicon oxynitride ($Si_xO_yN_z$) or silicon-rich oxide (Si_xO_y) where x, y, and z are real numbers. In some embodiments, cap layer 1440 includes hydrogenated silicon oxynitride ($Si_xO_yN_z$:H) or hydrogenated silicon-rich oxide (Si_xO_y:H). Layers 1440 and 1450 are formed using known techniques. Amorphous carbon layer 1330, cap layer 1440, and photoresist layer 1450 form a masking structure 1460. In some embodiments, cap layer 1440 is omitted from masking structure 1460. In other embodiments, masking structure 1460 further includes an additional layer formed between photoresist layer 1450 and cap layer 1440. The additional layer serves as an antireflective layer to further enhance the photo processing performance.

FIG. 15 shows device 1100 after photoresist layer 1450 is patterned. Patterning photoresist layer 1450 can be performed using known techniques. Patterned photoresist layer 1450 includes openings 1552.

FIG. 16 shows device 1100 after masking structure 1460 is patterned. Patterning masking structure 1460 can be performed by one or more etching steps. In some embodiments, cap layer 1440 and amorphous carbon layer 1330 are etched together in one etching step. In other embodiments, cap layer 1440 and amorphous carbon layer 1330 are etched separately in different etching steps. As shown in FIG. 16, after patterning, each of the patterned cap layer 1440 and the patterned amorphous carbon layer 1330 includes openings that are continuous and aligned with openings 1552 of photoresist layer 1450.

In some embodiments, after amorphous carbon layer 1330 is patterned, the combination of layers 1330, 1440, and 1450 of masking structure 1460 may remain and is used as a mask to etch the layers of device structure 1220. In other embodiments, after amorphous carbon layer 1330 is patterned, either photoresist layer 1450 or a combination of both photoresist layer 1450 and cap layer 1440 is removed. The remaining (not removed) layer, or layers, of masking structure 1220 is used as a mask to etch device structure 1220.

FIG. 17 shows device 1100 after device structure 1220 is etched. In embodiments represented by FIG. 16, both photoresist layer 1450 and cap layer 1440 are removed before device structure 1220 is etched. Amorphous carbon layer 1330 is used as a mask to etch the layers of device structure 1220. The etched device structure 1220 has openings 1701.

FIG. 18 shows device 1100 after amorphous carbon layer 1330 is removed. In some embodiments, amorphous carbon layer 1330 is removed using an ash process with oxygen plasma. In other embodiments, amorphous carbon layer 1330 is removed using an ash process with a combination of oxygen plasma and CF_4.

FIG. 19 shows device 1100 after other layers are formed using known techniques. In each of the openings 1552, a first conductive layer 1902 (1902.1 and 1902.2), a second conductive layer1904 (1904.1 and 1904.2), and a dielectric layer 1906 (1906.1 and 1906.2) are formed. Conductive layers 1902, 1904, dielectric layer 1906 and other elements form storage capacitors C1 and

C2. For example, in storage capacitor C1, conductive layer 1902.1, contact 1140.1, and diffusion region 1106.1 form a first capacitor plate (bottom plate); conductive layer 1902.2 forms a second capacitor plate (top plate); and dielectric layer 1906.1 is the capacitor dielectric. In some embodiments, conductive layers 1904 connect to a common cell plate of memory device 1100. The common cell plate is omitted from FIG. 19 for simplicity.

Memory device 1110 includes access transistors T1 and T2. Gate structure 1105.2 and diffusion regions 1106.1-1106.2 form access transistor T1. Gate structure 1105.3 and diffusion regions 1106.2-1106.3 form access transistor T2. Access transistor T1 and storage capacitor C1 form a memory CELL1. Access transistor T2 and storage capacitor C2 form a memory CELL2.

Memory cells CELL1 and CELL2 store data in form of charge in storage capacitors C1 and C2. The charges are transferred to and from doped regions 1106.1 and 1106.3 of capacitors C1 and C2 via contact 1140.2. In some embodiments, contact 1140.2 is a buried bit line contact, which connects to a bit line of memory device 1100.

In other embodiments, other elements having structures different from the structures of the layers 1902, 1904, and 1906 can be formed in openings 1701 (FIG. 17). For example, interconnects instead of capacitor plates can be formed in openings 1552 to connect diffusion regions 1106 to other parts of memory device 1100.

Memory device 1100 may be a dynamic random access memory (DRAM) device. Examples of DRAM devices include synchronous DRAM commonly referred to as SDRAM, SDRAM II, SGRAM (Synchronous Graphics Random Access Memory), DDR SDRAM (Double Data Rate SDRAM), DDR II SDRAM, DDR III SDRAM, GDDR III SDRAM (Graphic Double Data Rate), and Rambus DRAMs. Memory device 1100 includes other elements, which are not shown for clarity.

FIG. 20 shows a system according to an embodiment of the invention. System 2000 includes a chamber 2010 and a wafer 2020 placed in the chamber. In some embodiments, chamber 2010 is a PECVD chamber and wafer 2020 is a semiconductor wafer. An example of chamber 2010 includes a chamber of the Producer Processor available from Applied Materials, Inc. located in Santa

Clara, California. Chamber 2010 and wafer 2020 can be used in method 100 described in FIG. 1A to form the transparent amorphous carbon layer according to method 100.

Wafer 2020 includes a number of alignment marks 2014 and a number of dice 2030. In some embodiments, alignment marks 2014 represent alignment marks 214 (FIG. 2) and alignment marks 1104 (FIG. 11).

At least one of the dice 2030 includes elements according to embodiments described in FIG. 2-FIG. 19 above. For example, at least one of the dice 2030 includes a substrate, a device structure, and a masking structure such as those of devices 200 and 1100 (FIG. 2-FIG. 19). Thus, at least one of the dice 2030 includes an amorphous carbon layer such as amorphous carbon layer 430 (FIG. 4A) and amorphous carbon layer 1330 (FIG. 13) formed according to the process described in FIG. 2-FIG. 19.

A die such as one of the dice 2030 is a pattern on a semiconductor wafer such as wafer 2020. A die contains circuitry to perform a specific function. For, example, at least one of the dice 2030 contains circuitry for a device such as a processor, or memory device such as memory device 1100 (FIG. 11-FIG. 19).

Conclusion

Various embodiments of the invention provide technique to form a transparent amorphous carbon layer. The transparent amorphous carbon layer can be used as a mask for etching certain structure of the device. The amorphous carbon layer can also be a part of a structure of the device for other purposes. Although specific embodiments are described herein, those skilled in the art recognize that other embodiments may be substituted for the specific embodiments shown to achieve the same purpose. This application covers any adaptations or variations of the present invention. Therefore, the present invention is limited only by the claims and all available equivalents.

What is claimed is:

1. A device in a process, the device comprising:
a substrate;
a device structure formed over the substrate; and
a masking structure formed over the device structure, the masking structure including an amorphous carbon layer, wherein the amorphous carbon layer is transparent in visible light range.

2. The device of claim 1, wherein the amorphous carbon layer has an absorption coefficient between about 0.15 and about 0.001 at wavelength of 633 nanometers.

3. The device of claim 1, wherein the visible light range includes electromagnetic radiation having wavelengths between 400 nanometers and 700 nanometers.

4. The device of claim 1, wherein the amorphous carbon layer has a thickness greater than 4000 Angstroms.

5. The device of claim 4, wherein the device structure has a thickness greater than 40000 Angstroms.

6. The device of claim 1, wherein the masking structure further includes a silicon oxynitride layer formed over the amorphous carbon layer.

7. The device of claim 1, wherein the masking structure further includes a photoresist layer.

8. The device of claim 7, wherein the masking structure further includes an antireflective layer.

9. The device of claim 7 wherein the photoresist layer includes at least one opening.

10. The device of claim 9, wherein the amorphous carbon layer includes at least one opening continuous with the at least one opening of the photoresist layer.

11. The device of claim 1, wherein the device structure includes a layer selected from a material in a group consisting of a conducting material, a non-conducting material, and a semiconducting material.

12. The device of claim 11, wherein the device structure further includes an amorphous carbon layer, wherein the amorphous carbon layer of the device structure is transparent in visible light range.

13. A mask structure for a device, the mask structure comprising:

an amorphous carbon layer, wherein the amorphous carbon layer is transparent to radiation having wavelengths between 400 nanometers and 700 nanometers.

14. The mask structure of claim 13, wherein the amorphous carbon layer has an absorption coefficient between about 0.15 and about 0.001 at wavelength of 633 nanometers.

15. The mask structure of claim 13, wherein the amorphous carbon layer has a thickness of at least 4000 Angstroms.

16. The mask structure of claim 13 further comprising a photoresist layer.

17. The mask structure of claim 16 further comprising a cap layer formed over the amorphous carbon layer.

18. The mask structure of claim 17, wherein the a cap layer includes silicon oxynitride.

19. The mask structure of claim 16, wherein the photoresist layer includes at least one opening.

20. The mask structure of claim 19, wherein the amorphous carbon layer includes at least one opening continuous with the at least one opening of the photoresist layer.

21. A memory device in a process, the memory device comprising:

a substrate having a plurality of doped regions;

device structure formed over the substrate, the device structure including a plurality of gate structures, a plurality of contacts, each of the contacts being located between two gate structure and contacting one of the doped regions, and an insulating layer formed over the gate structures and the contacts; and

a masking structure formed over the device structure, the masking structure including an amorphous carbon layer, wherein the amorphous carbon layer is transparent in visible light range.

22. The memory device of claim 21, wherein the amorphous carbon layer has a thickness of at least 4000 Angstroms.

23. The memory device of claim 22, wherein the device structure has a thickness of at least 40000 Angstroms.

24. The memory device of claim 21, wherein the masking structure further includes a silicon oxynitride layer formed over the amorphous carbon layer.

25. The memory device of claim 21, wherein the masking structure further includes a photoresist layer.

26. The memory device of claim 25, wherein the masking structure further includes an antireflective layer.

27. The memory device of claim 25, wherein the photoresist layer includes at least one opening of the photoresist layer.

28. The memory device of claim 27, wherein the amorphous carbon layer includes at least one opening continuous with the at least one opening of the photoresist layer.

29. The memory device of claim 28, wherein the insulating layer includes at least one opening continuous with both of the at least one opening of the amorphous carbon layer and the at least one opening of the photoresist layer.

30. The memory device of claim 21, wherein the device structure further includes a barrier layer located between the gate structures and the contacts.

31. The memory device of claim 21, wherein the amorphous carbon layer has an absorption coefficient between about 0.15 and about 0.001 at wavelength of 633 nanometers.

32. A system comprising:

a chamber having a temperature between about 200°C and about 500°C; and

a wafer place in the chamber, the wafer including a die, the die including a substrate, a device structure formed over the substrate, and a masking structure formed over the device structure, the masking structure including an amorphous carbon layer, wherein the amorphous carbon layer is transparent in visible light range.

33. The system of claim 32, wherein the amorphous carbon layer has a thickness greater than 4000 Angstroms.

34. The system of claim 33, wherein the device structure has a thickness greater than 40000 Angstroms.

35. The system of claim 34, wherein the masking structure further includes a silicon oxynitride layer formed over the amorphous carbon layer.

36. The system of claim 32, wherein the masking structure further includes a photoresist layer.

37. The system of claim 36, wherein the masking structure further includes an antireflective layer.

38. The system of claim 36, wherein the photoresist layer includes at least one opening.

39. The system of claim 38, wherein the amorphous carbon layer includes at least one opening continuous with the at least one opening of the photoresist layer.

40. The system of claim 32, wherein the device structure includes a conductive layer.

41. The system of claim 40, wherein the device structure further includes an insulating layer.

42. The system of claim 41, wherein the device structure further includes an antireflective layer.

43. The system of claim 42, wherein the device structure further includes an amorphous carbon layer.

44. The system of claim 43, wherein the masking structure further includes a photoresist layer.

45. The system of claim 44, wherein the masking structure further includes an antireflective layer.

46. The system of claim 32, wherein the at least one die includes circuitry for a memory device.

47. The system of claim 32, wherein the at least one die includes circuitry for a processor.

48. The system of claim 32, wherein the chamber is a plasma enhanced vapor chemical deposition chamber.

49. A method comprising:

forming a device structure over a substrate; and

forming a masking structure over the substrate including forming an amorphous carbon layer, wherein the amorphous carbon layer is transparent in visible light range.

50. The method of claim 49, wherein forming an amorphous carbon layer includes forming the amorphous carbon layer having a thickness of at least 4000 Angstroms.

51. The method of claim 50, wherein forming the device structure including forming the device structure having a thickness of at least 40000 Angstroms.

52. The method of claim 49, wherein forming the masking structure further includes forming a silicon oxynitride layer over the amorphous carbon layer.

53. The method of claim 52, wherein the silicon oxynitride layer is in situ deposited together with the amorphous carbon layer.

54. The method of claim 49, wherein forming an amorphous carbon layer includes patterning the amorphous carbon layer to form a patterned amorphous carbon layer.

55. The method of claim 54, wherein forming a device structure includes patterning the device structure using the patterned amorphous carbon layer as a mask.

56. The method of claim 49, wherein forming a masking structure further includes forming a patterned photoresist layer.

57. The method of claim 56, wherein forming a masking structure further includes patterning the amorphous carbon layer using the patterned photoresist layer as a mask.

58. The method of claim 56, wherein forming a device structure includes patterning the device structure using the patterned amorphous carbon layer as a mask.

59. The method of claim 49, wherein the amorphous carbon layer has an absorption coefficient between about 0.15 and about 0.001 at wavelength of 633 nanometers.

60. The method of claim 59, wherein the amorphous carbon is formed at a temperature range of about 200°C to about 500°C.

61. The method of claim 49, wherein the visible light range includes electromagnetic radiation having wavelengths between 400 nanometers and 700 nanometers.

62. A method comprising:

forming a device structure over a substrate; and

forming a masking structure over the device structure including forming an amorphous carbon layer at a temperature range of about 200°C to about 500°C.

63. The method of claim 62, wherein forming the masking structure further includes forming a silicon oxynitride layer over the amorphous carbon layer.

64. The method of claim 63, wherein the silicon oxynitride layer is in situ deposited together with the amorphous carbon layer.

65. The method of claim 64, wherein the amorphous carbon layer has an absorption coefficient between about 0.15 and about 0.001 at wavelength of 633 nanometers.

66. The method of claim 62, wherein forming an amorphous carbon layer includes forming the amorphous carbon layer at a temperature from about 200°C to about below 300°C.

67. The method of claim 62, wherein forming an amorphous carbon layer includes forming the amorphous carbon layer having a thickness greater than 4000 Angstroms.

68. The method of claim 67, wherein forming the device structure includes forming the device structure having a thickness greater than 40000 Angstroms.

69. The method of claim 62, wherein forming an amorphous carbon layer is performed in a chamber subjected to a pressure range of about 4 Torr to about 6.5 Torr, a radio frequency power range of about 450 Watts to about 1000 Watts, and a gas mixture including propylene.

70. The method of claim 69, wherein the gas mixture further includes helium.

71. The method of claim 70, wherein the propylene is introduced into the chamber at a flow rate of between 500 standard cubic centimeters per minute (sccm) and 4000 sccm.

72. The method of claim 71, wherein the helium is introduced into the chamber at a flow rate of between 250 sccm and 1000 sccm.

73. A method comprising:

forming a device structure on a substrate;

forming a making structure over the device structure including forming an amorphous carbon layer, wherein the amorphous carbon layer is transparent in visible light range; and

etching the device structure using the amorphous carbon layer as a mask.

74. The method of claim 73, wherein forming an amorphous carbon layer is performed in a chamber with a temperature range of about 200°C to about 500°C, a pressure range of about 4 Torr to about 6.5 Torr, a radio frequency power range of about 450 Watts to about 1000 Watts, and a mixture of gas including propylene.

75. The method of claim 74, wherein the propylene is introduced into the chamber at a flow rate between 500 standard cubic centimeters per minute (sccm) and 4000 sccm.

76. The method of claim 75, wherein the helium is introduced into the chamber at a flow rate between 250 sccm and 1000 sccm.

77. The method of claim 73, wherein forming an amorphous carbon layer is performed by a chemical vapor deposition process.

78. The method of claim 73, wherein forming the masking structure further includes forming a silicon oxynitride layer over the amorphous carbon layer.

79. The method of claim 78, wherein the silicon oxynitride layer is in situ deposited together with the amorphous carbon layer.

80. The method of claim 79, wherein the amorphous carbon layer has an absorption coefficient between about 0.15 and about 0.001 at wavelength of 633 nanometers.

81. A method comprising:

forming an amorphous carbon layer in which the amorphous carbon layer is transparent in visible light range, wherein forming an amorphous carbon layer is performed in a chamber with a temperature above 200°C and below 500°C, a pressure range of about 4 Torr to about 6.5 Torr, an radio frequency power range of about 450 Watts to about 1000 Watts, and a mixture of gas including propylene.

82. The method of claim 81, wherein forming an amorphous carbon layer includes forming the amorphous carbon layer having a thickness greater than 4000 Angstroms.

83. The method of claim 81, wherein the mixture of gas further includes helium.

84. The method of claim 83, wherein the propylene is introduced into the chamber at a flow rate of between 500 standard cubic centimeters per minute (sccm) and 4000 sccm.

85. The method of claim 84, wherein the helium is introduced into the chamber at a flow rate of between 250 sccm and 1000 sccm.

86. A method comprising:

forming device structure having a gate structure on a substrate;

forming an amorphous carbon layer over the device structure, wherein the an amorphous carbon layer is transparent in visible light range;

patterning the amorphous carbon layer to form a patterned amorphous carbon layer;

etching the device structure using the patterned amorphous carbon layer as a mask to form a structure of a capacitor of a memory cell; and

removing the patterned amorphous carbon layer.

87. The method of claim 86, wherein patterning the amorphous carbon layer includes:

forming a patterned photoresist layer over the amorphous carbon layer; and

etching the amorphous carbon layer using the patterned photoresist layer as a mask.

88. The method of claim 87 further comprising:

forming a silicon oxynitride layer over the over the amorphous carbon layer before forming the patterned photoresist layer.

89. The method of claim 88, wherein the silicon oxynitride layer is in situ deposited together with the amorphous carbon layer.

90. The method of claim 86, wherein removing the patterned amorphous carbon is performed using an oxygen plasma process.

91. The method of claim 86, wherein removing the patterned amorphous carbon is performed using an oxygen plasma process with one of CF_4 and H_2.

92. A method comprising:

placing a wafer in a chamber, the wafer including at least one die having a substrate and a device structure formed over the substrate;

setting a temperature in the chamber between about 200°C and about 500°C; and

forming a masking structure over the device structure including forming an amorphous carbon layer.

93. The method of claim 92, wherein forming the masking structure further includes forming a silicon oxynitride layer over the amorphous carbon layer.

94. The method of claim 93, wherein the silicon oxynitride layer is in situ deposited together with the amorphous carbon layer.

95. The method of claim 94, wherein the amorphous carbon layer has an absorption coefficient between about 0.15 and about 0.001 at wavelength of 633 nanometers.

96. The method of claim 92, wherein forming an amorphous carbon layer is performed until the amorphous carbon layer has a thickness of at least 4000 Angstroms.

97. The method of claim 92 further comprising:

introducing a propylene into the chamber;

setting a pressure in the chamber between about 4 Torr and about 6.5 Torr; and

subjecting the wafer to a power between about 450 Watts and about 1000 Watts.

98. The method of claim 92 further comprising:

introducing helium into the chamber.

99. The method of claim 98, wherein the propylene is introduced into the chamber at a flow rate between 500 standard cubic centimeters per minute (sccm) and 4000 sccm.

100. The method of claim 99, wherein the helium introduced into the chamber at a flow rate between 250 sccm and 1000 sccm.

101. The method of claim 92, wherein the chamber is a plasma enhanced vapor chemical deposition chamber.

102. A method comprising:

forming a number of memory cells including forming an amorphous carbon layer, wherein the amorphous carbon layer is transparent in visible light range.

103. The method of claim 102, wherein forming a number of memory cells further includes forming a silicon oxynitride layer over the amorphous carbon layer.

104. The method of claim 103, wherein the silicon oxynitride layer is in situ deposited together with the amorphous carbon layer.

105. The method of claim 104, wherein the amorphous carbon layer has an absorption coefficient between about 0.15 and about 0.001 at wavelength of 633 nanometers.

106. The method of claim 102, wherein amorphous carbon layer a thickness of at least 4000 Angstroms.

107. The method of claim 102, wherein forming a number of memory cells includes:

forming a number of transistors; and

forming a number of capacitors having a capacitor plate.

108. The method of claim 107, wherein the capacitor plate is formed after using the amorphous carbon layer to etch an insulating layer over gate structures of the transistors.

109. The method of claim 108, wherein the layer is performed in a chamber with a temperature range of about 200°C to about 500°C, a pressure range of

about 4 Torr to about 6.5 Torr, an radio frequency power range of about 450 Watts to about 1000 Watts, and a mixture of gas including propylene.

110. The method of claim 109, wherein the mixture of gas further includes helium.

111. The method of claim 110, wherein the propylene is introduced into the chamber at a flow rate between 500 standard cubic centimeters per minute (sccm) and 4000 sccm.

112 The method of claim 112, wherein the helium is introduced into the chamber at a flow rate between 250 sccm and 1000 sccm.

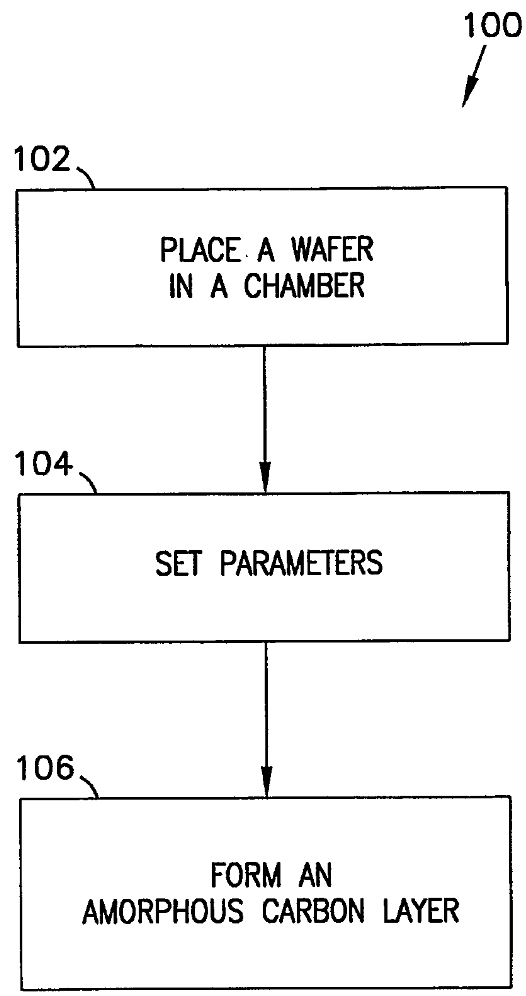

100
102
PLACE A WAFER IN A CHAMBER
104
SET PARAMETERS
106
FORM AN AMORPHOUS CARBON LAYER

FIG. 1A

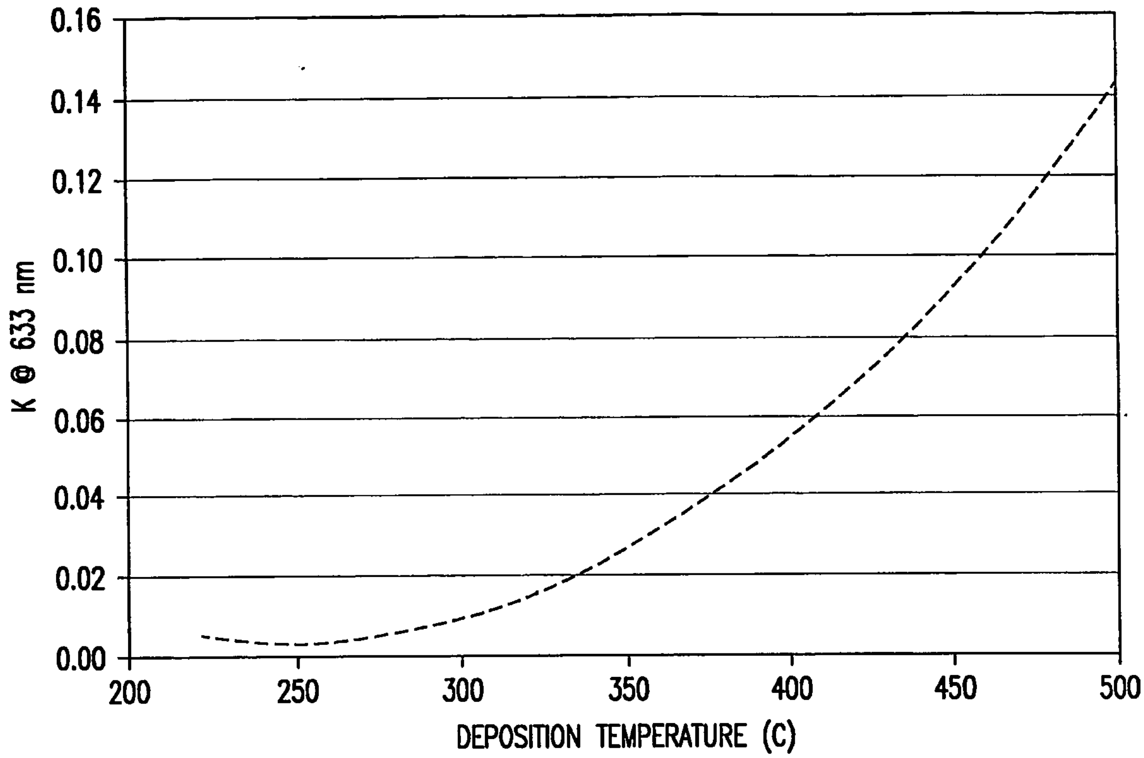

0.16
0.14
0.12
0.10
0.08
0.06
0.04
0.02
0.00
K @ 633 nm
200
250
300
350
400
450
500
DEPOSITION TEMPERATURE (C)

FIG. 1B

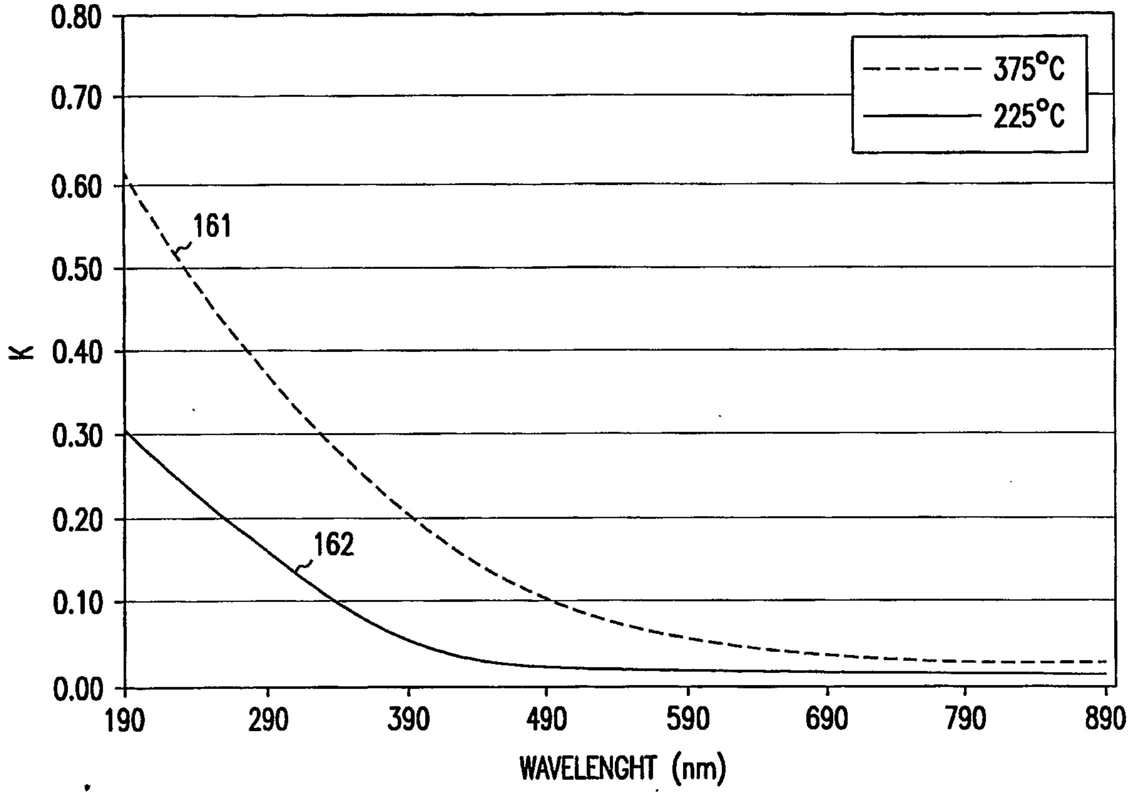

0.80
0.70
0.60
0.50
0.40
0.30
0.20
0.10
0.00
K
190
290
390
490
590
690
790
890
WAVELENGHT (nm)
375°C
225°C
161
162

FIG. 1C

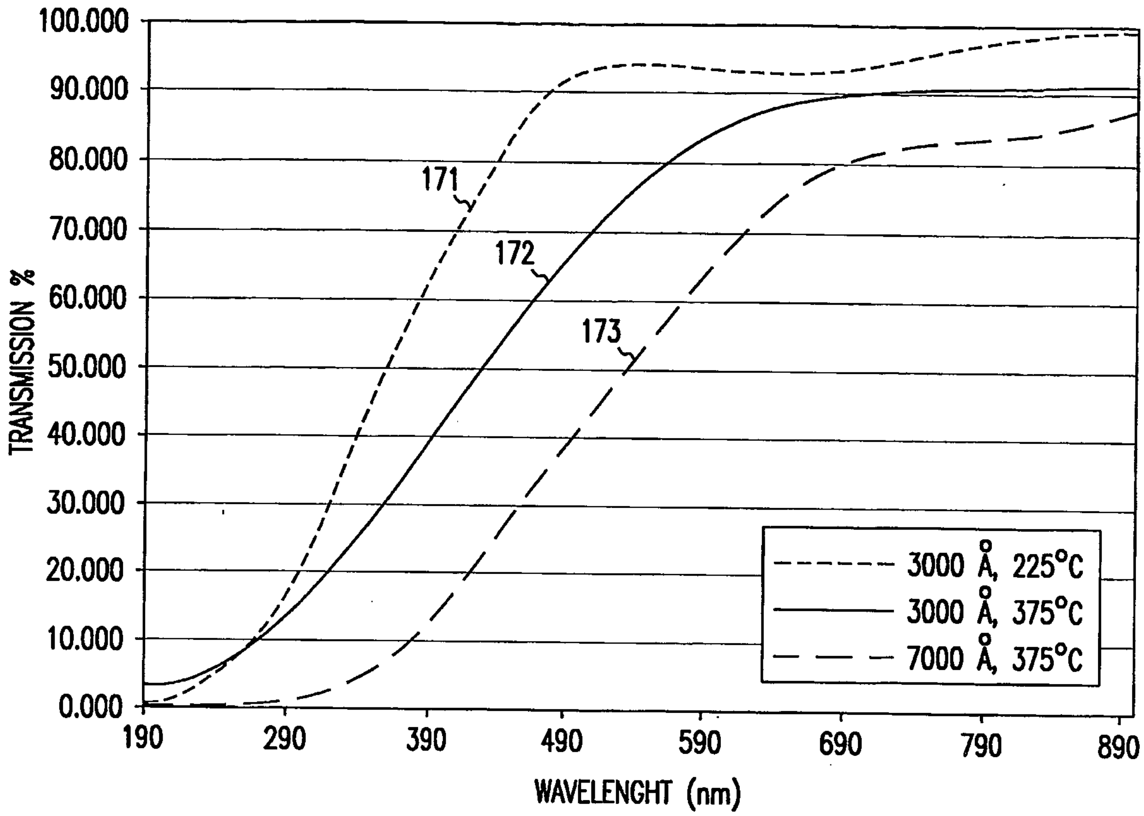

100.000
90.000
80.000
70.000
60.000
50.000
40.000
30.000
20.000
10.000
0.000
TRANSMISSION %
190
290
390
490
590
690
790
890
WAVELENGHT (nm)
171
172
173
3000 Å, 225°C
3000 Å, 375°C
7000 Å, 375°C

FIG. 1D

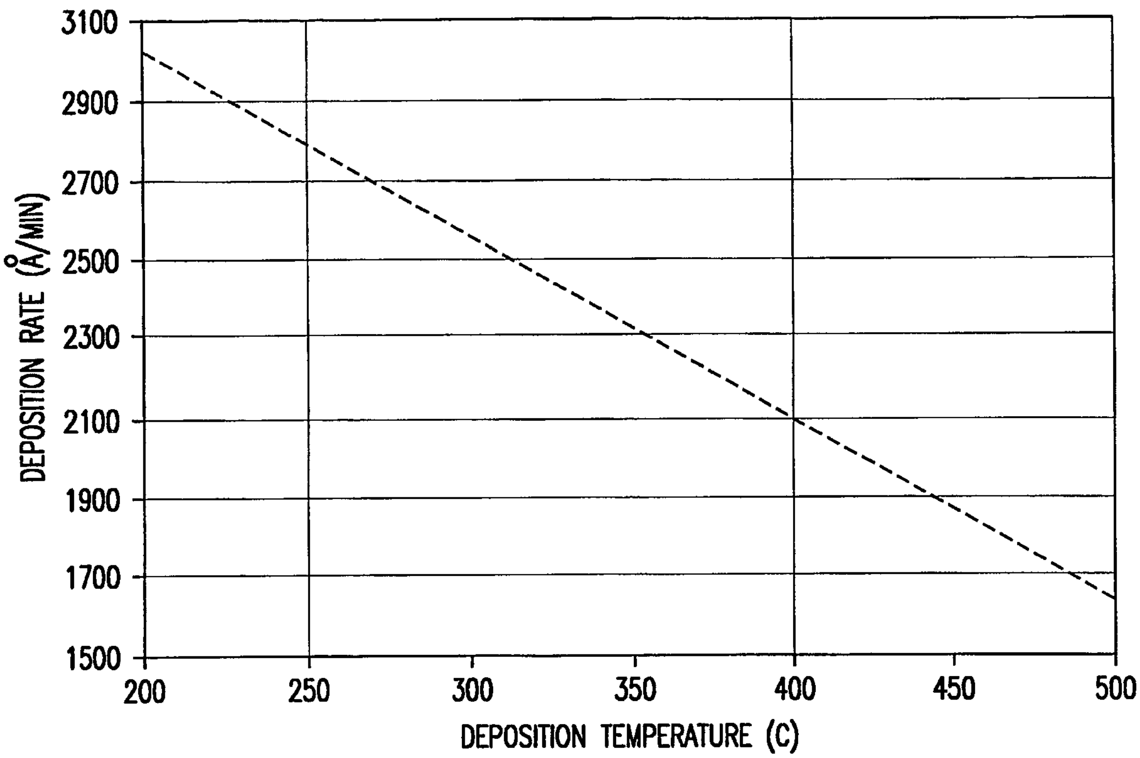

3100
2900
2700
2500
2300
2100
1900
1700
1500
DEPOSITION RATE (Å/MIN)
200
250
300
350
400
450
500
DEPOSITION TEMPERATURE (C)

FIG. 1E

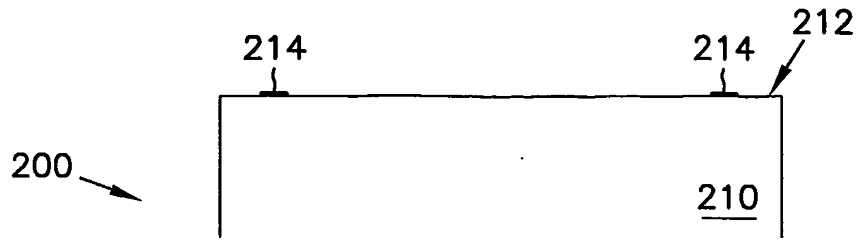


FIG. 2

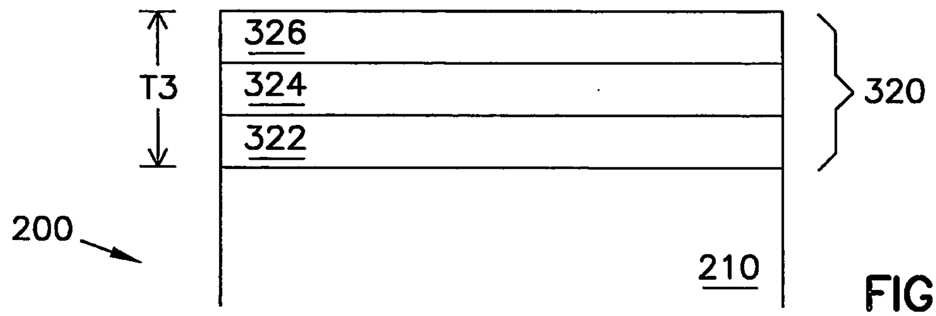


FIG. 3

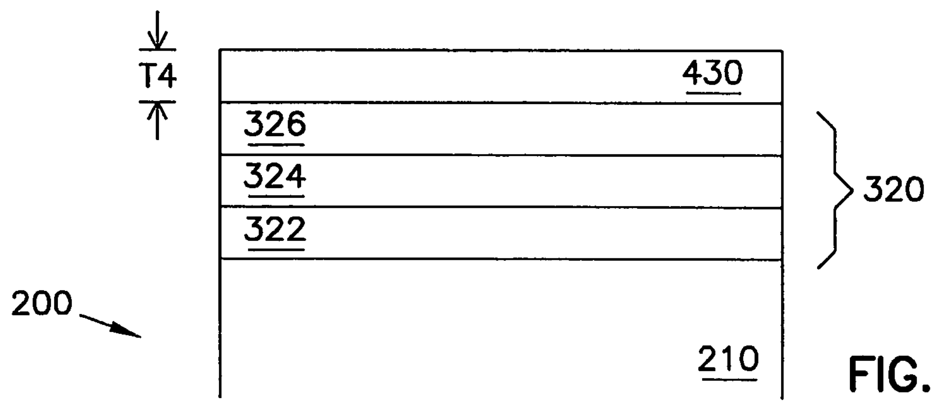


FIG. 4A

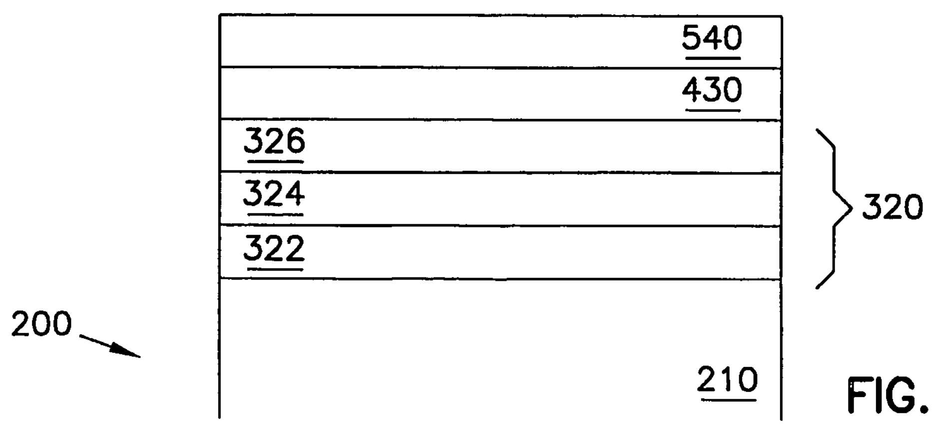


FIG. 4B

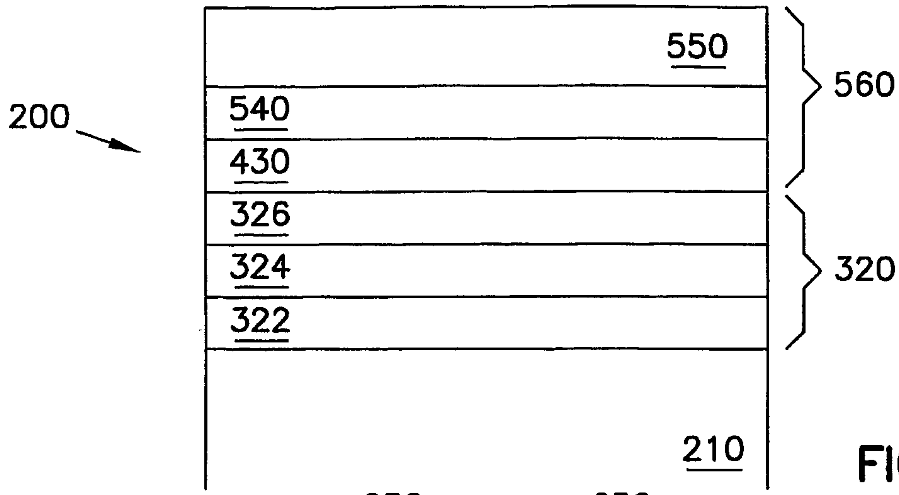


FIG. 5

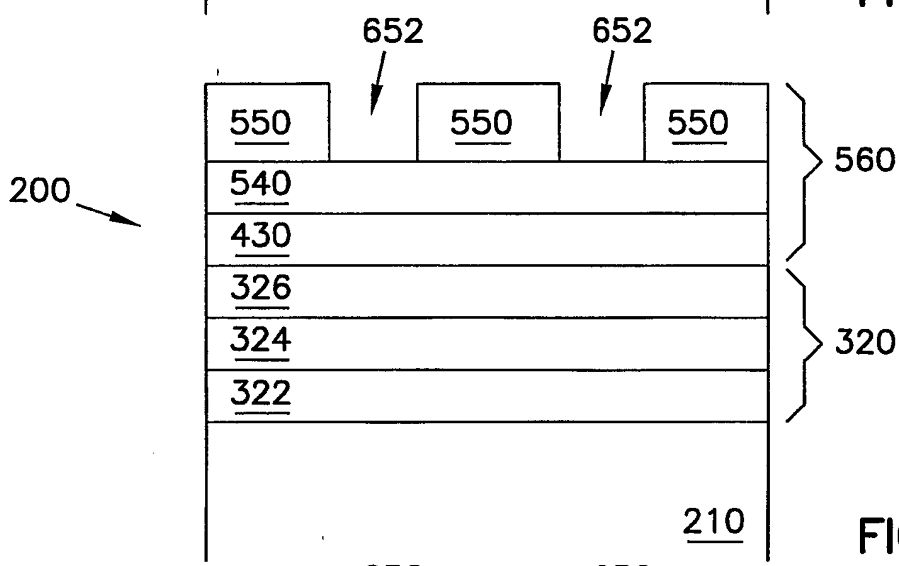


FIG. 6

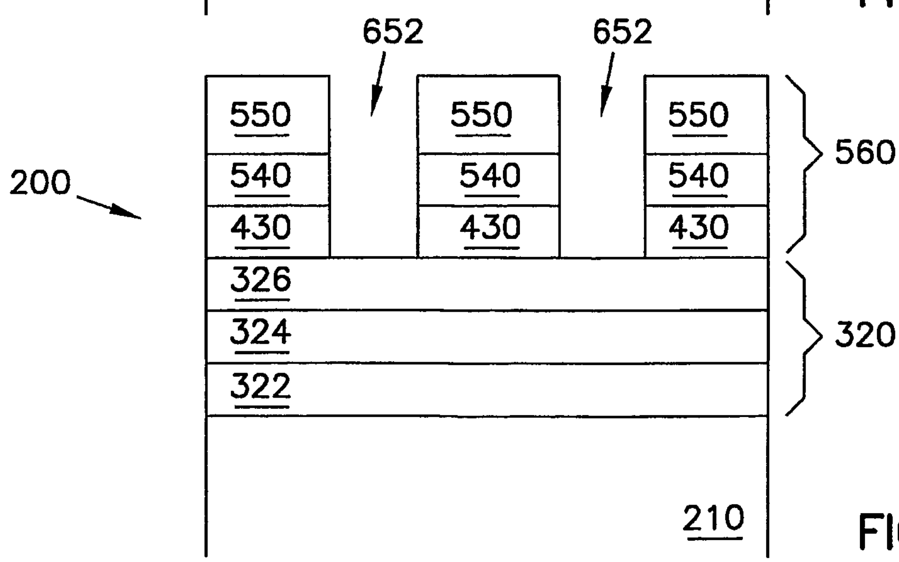


FIG. 7

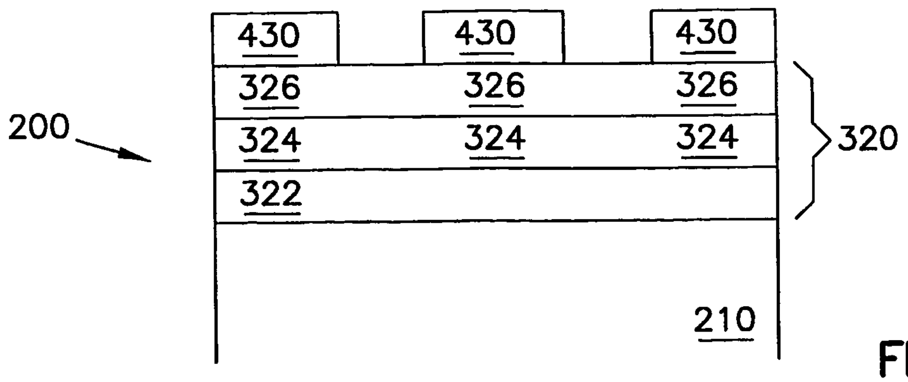


FIG. 8

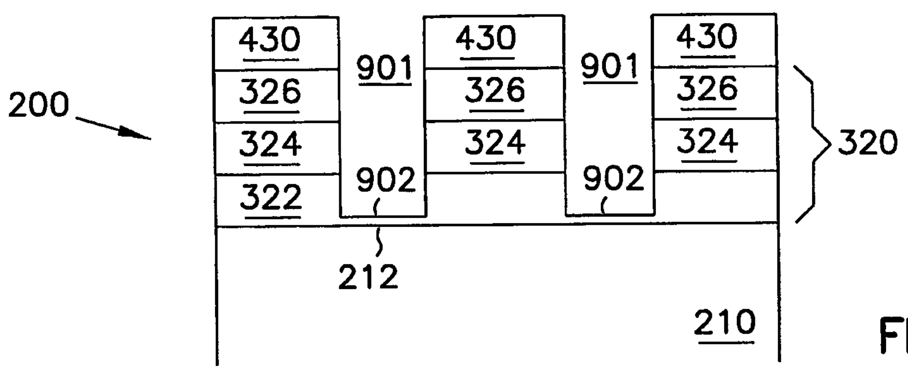


FIG. 9

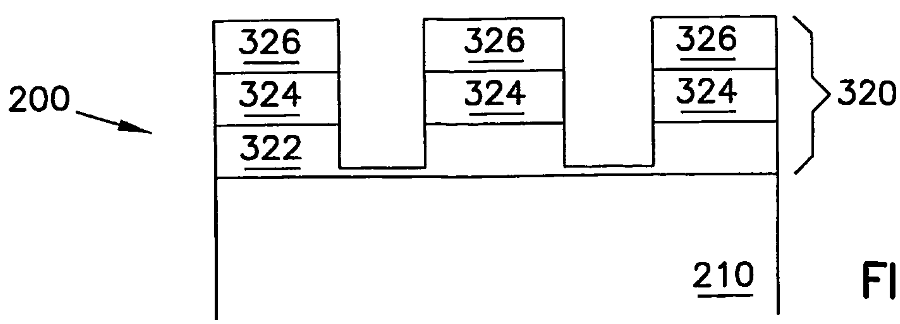


FIG. 10

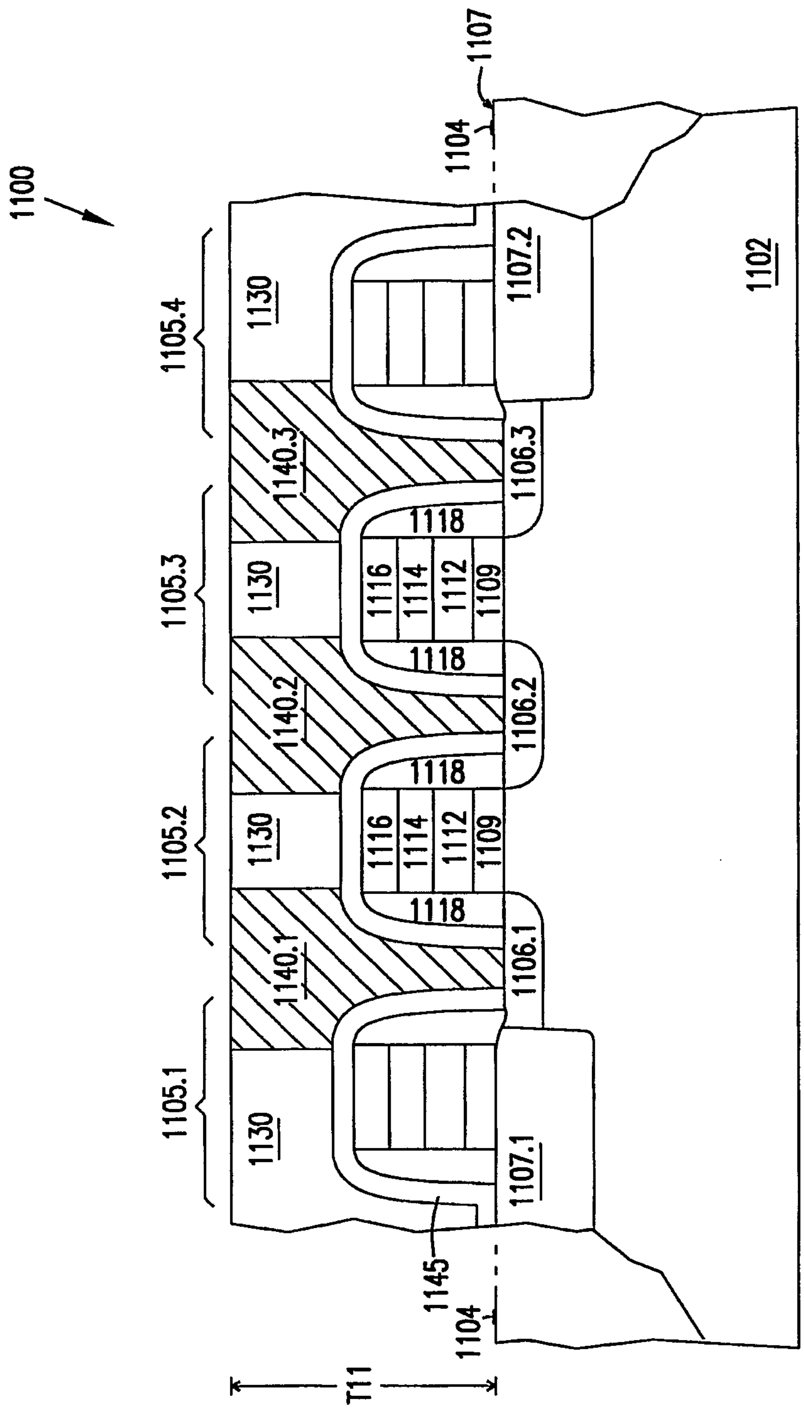
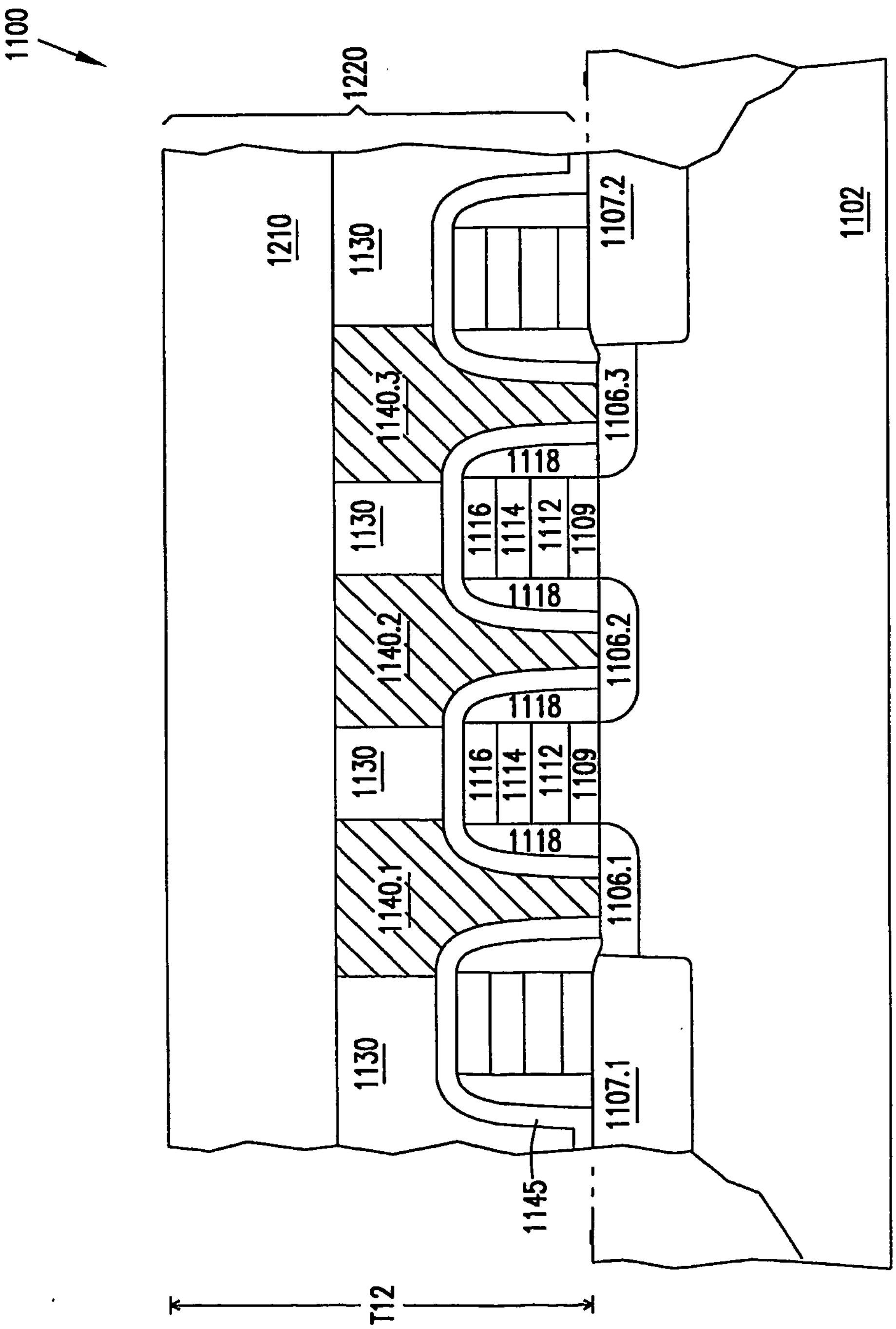

1100
1107
1104
1105.4
1130
1107.2
1102
1140.3
1106.3
1105.3
1118
1116
1114
1112
1109
1140.2
1106.2
1105.2
1140.1
1106.1
1105.1
1107.1
1145
T11

FIG. 11


1100
1220
1210
1130
1107.2
1102
1140.3
1106.3
1118
1116
1114
1112
1109
1130
1118
1140.2
1106.2
1118
1130
1116
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1112
1109
1118
1140.1
1106.1
1130
1107.1
1145
T12

FIG. 12

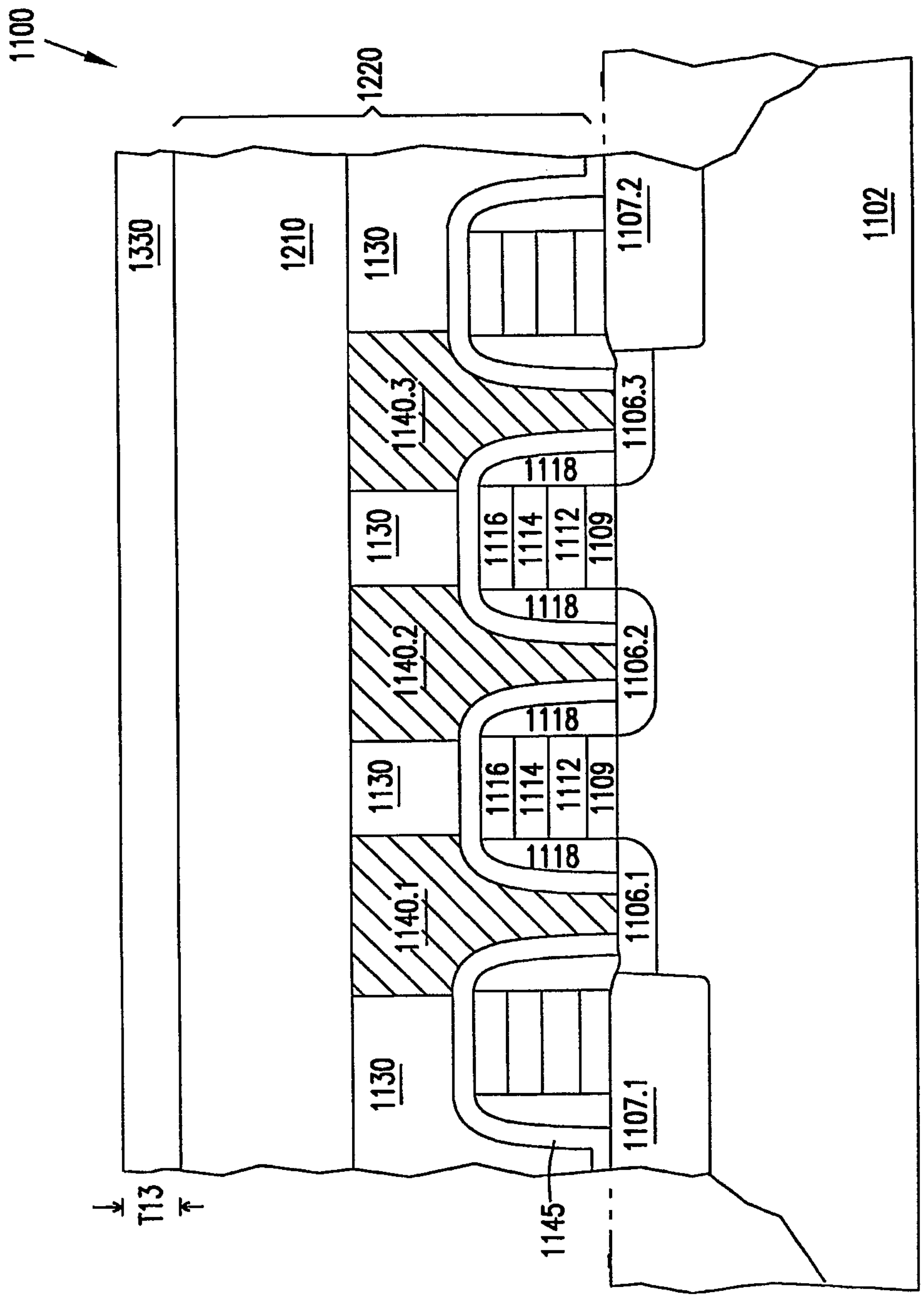

1100
1220
1330
1210
1130
1107.2
1102
1140.3
1106.3
1118
1116
1114
1112
1109
1140.2
1106.2
1140.1
1106.1
1107.1
1145
T13

FIG. 13

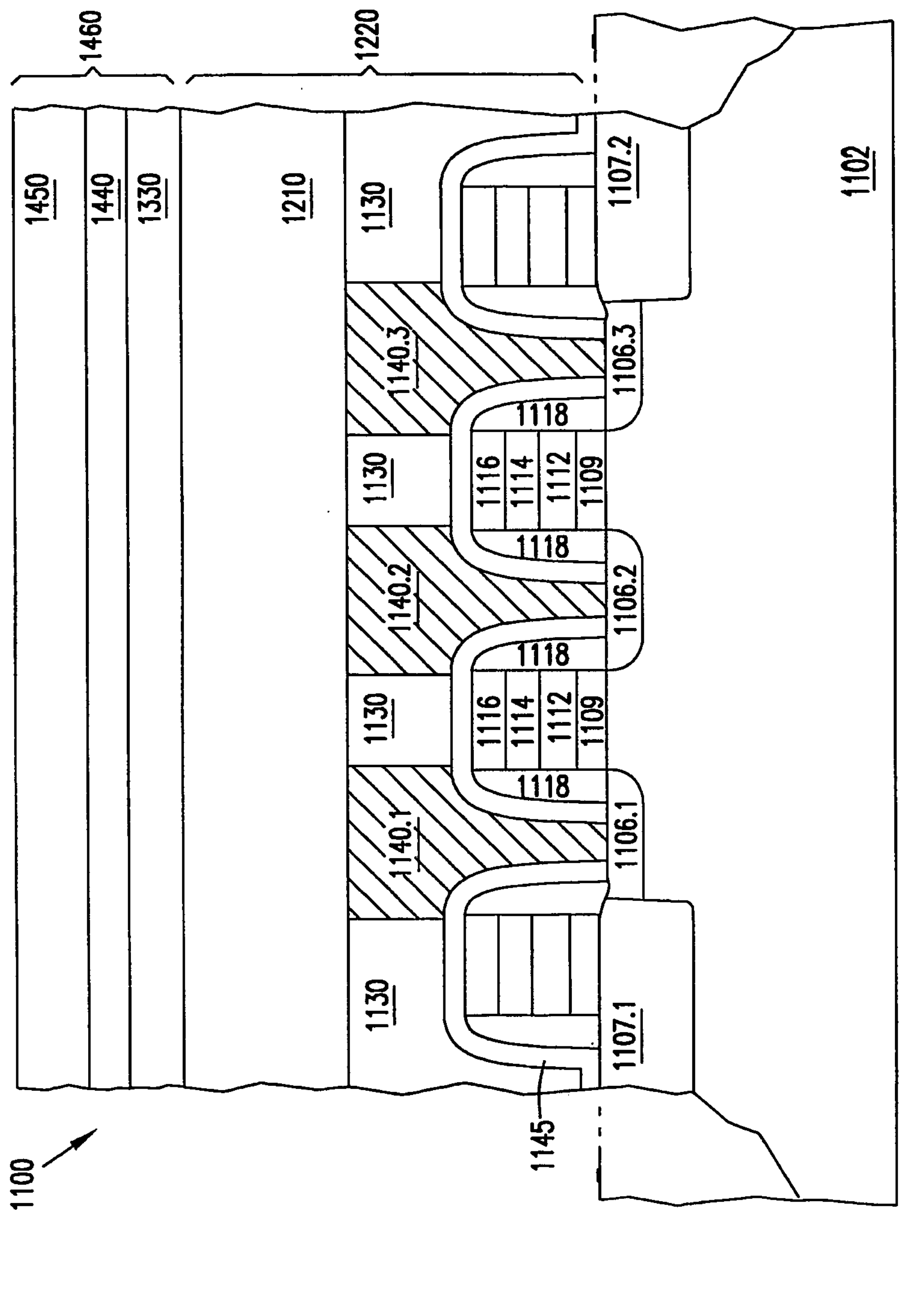

1460
1220
1450
1440
1330
1210
1130
1107.2
1102
1140.3
1106.3
1118
1116
1114
1112
1109
1140.2
1106.2
1140.1
1106.1
1107.1
1145
1100

FIG. 14

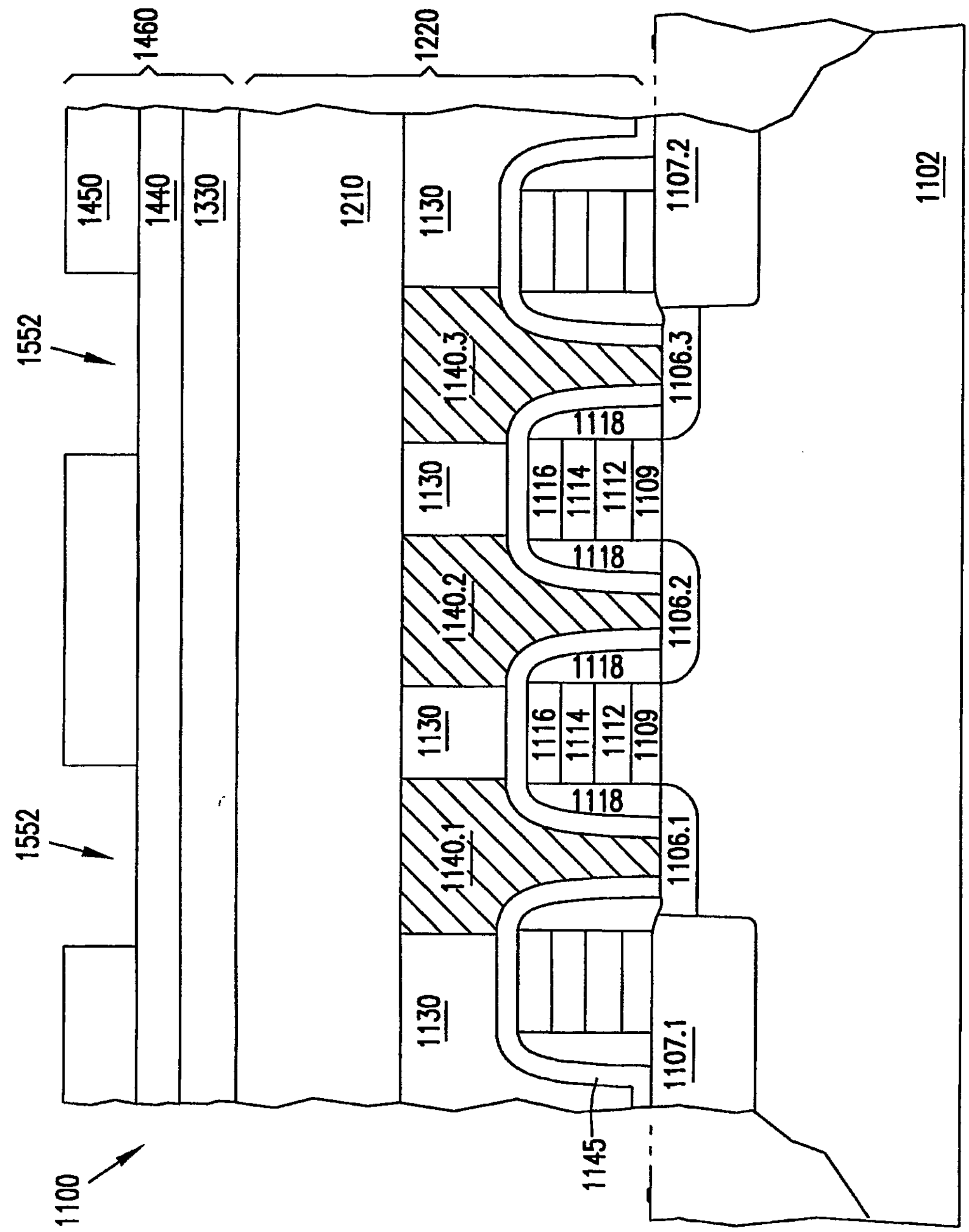
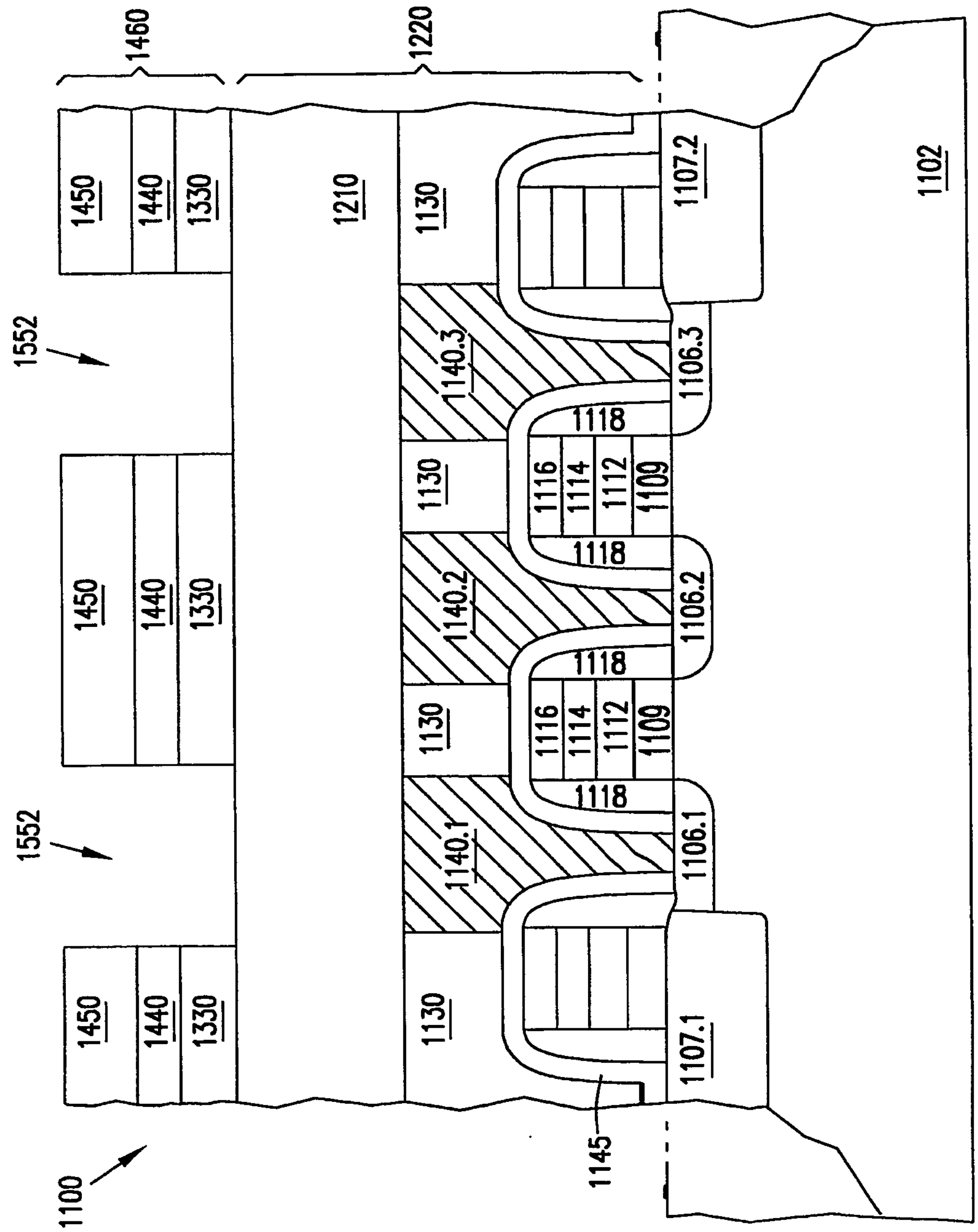

1460
1220
1450
1440
1330
1210
1130
1107.2
1102
1552
1140.3
1106.3
1118
1116
1114
1112
1109
1130
1118
1140.2
1106.2
1118
1130
1116
1114
1112
1109
1118
1552
1140.1
1106.1
1130
1107.1
1145
1100

FIG. 15


1460
1220
1450
1440
1330
1450
1440
1330
1450
1440
1330
1552
1552
1210
1130
1130
1130
1130
1140.3
1140.2
1140.1
1118
1116
1114
1112
1109
1118
1118
1116
1114
1112
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1118
1107.2
1106.3
1106.2
1106.1
1107.1
1102
1145
1100

FIG. 16

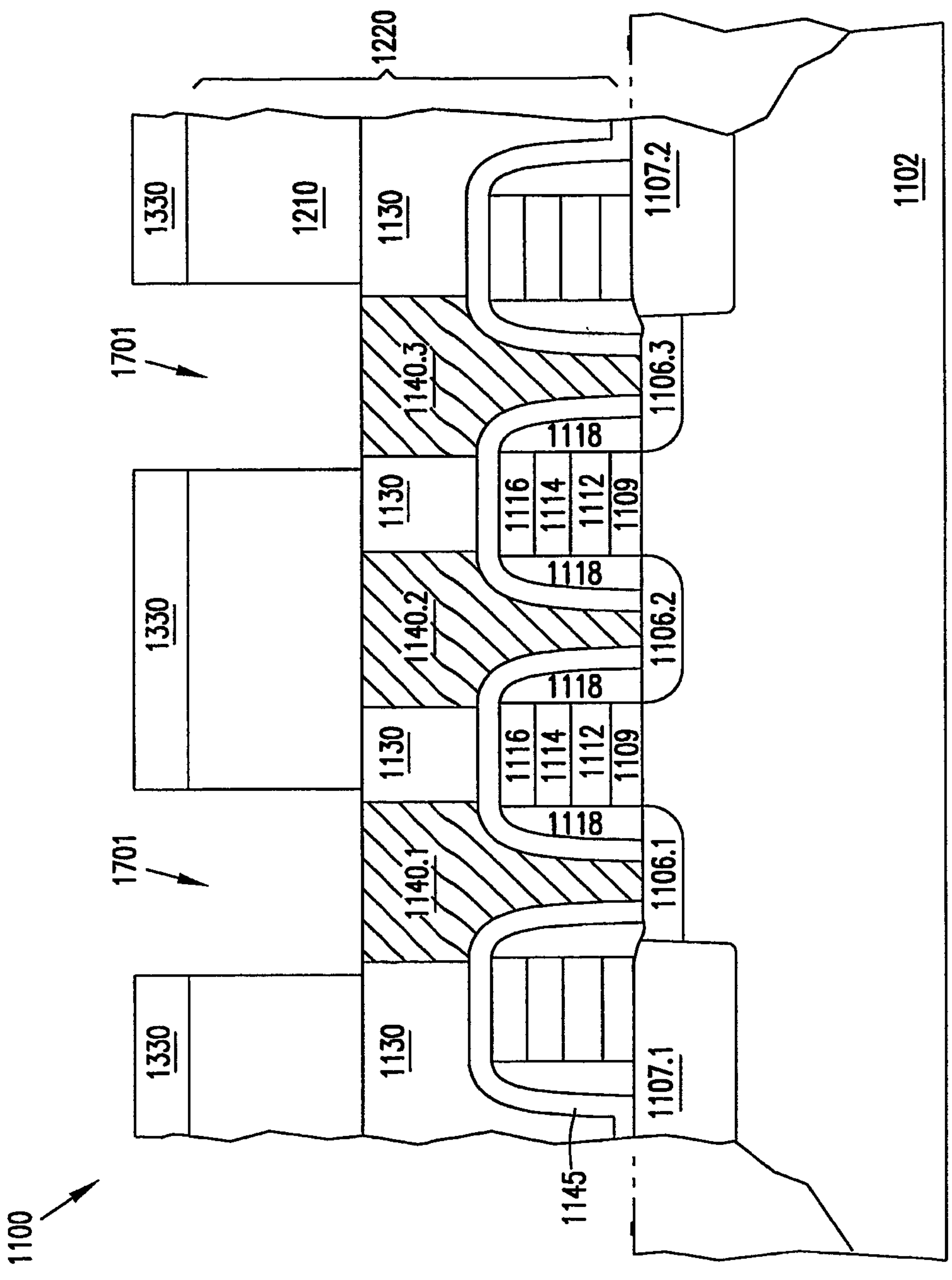
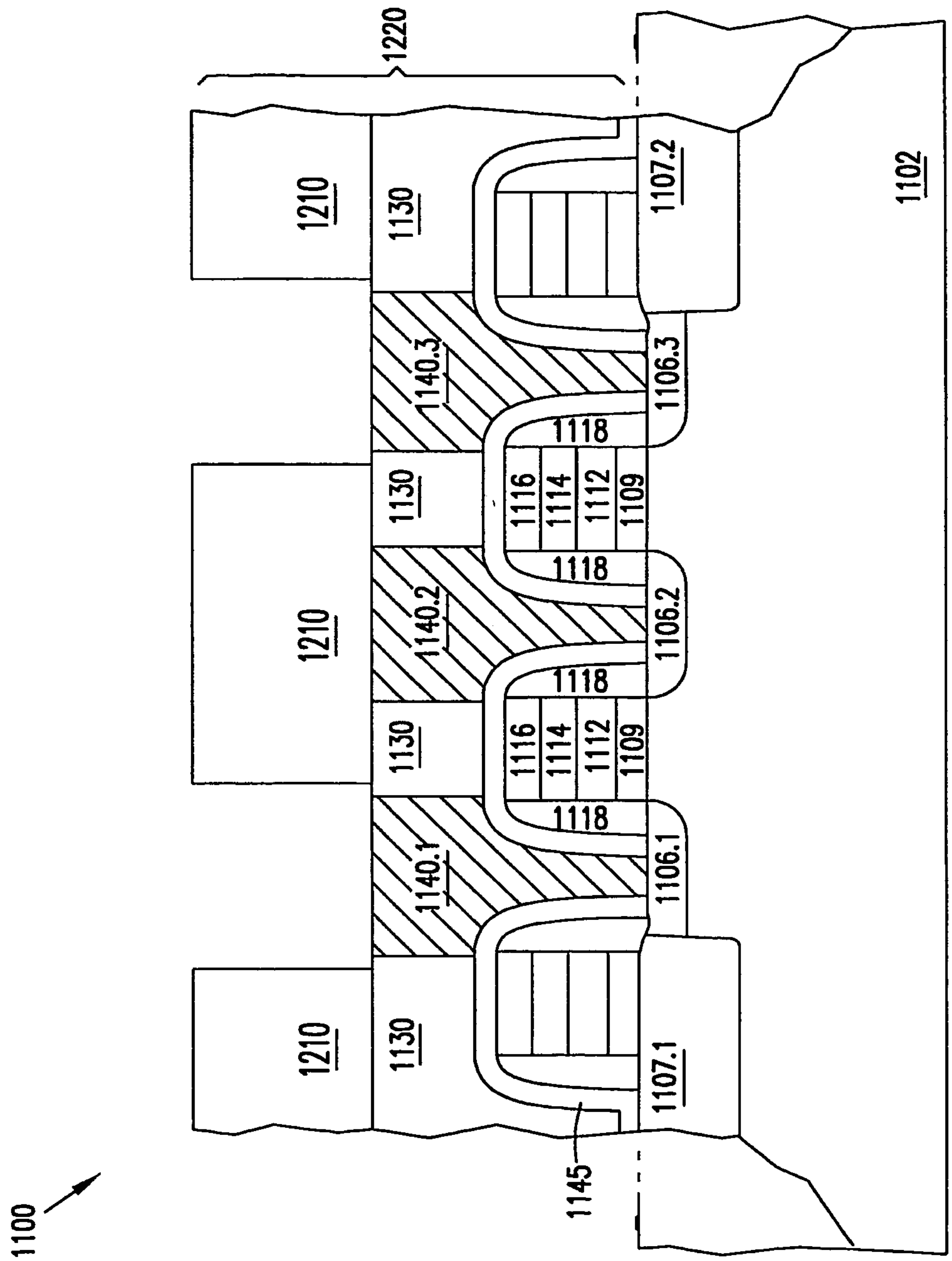

1220
1330
1210
1130
1107.2
1102
1701
1140.3
1106.3
1118
1116
1114
1112
1109
1140.2
1106.2
1140.1
1106.1
1107.1
1145
1100

FIG. 17



1220
1210
1130
1107.2
1102
1140.3
1106.3
1118
1116
1114
1112
1109
1140.2
1106.2
1140.1
1106.1
1107.1
1145
1100

FIG. 18

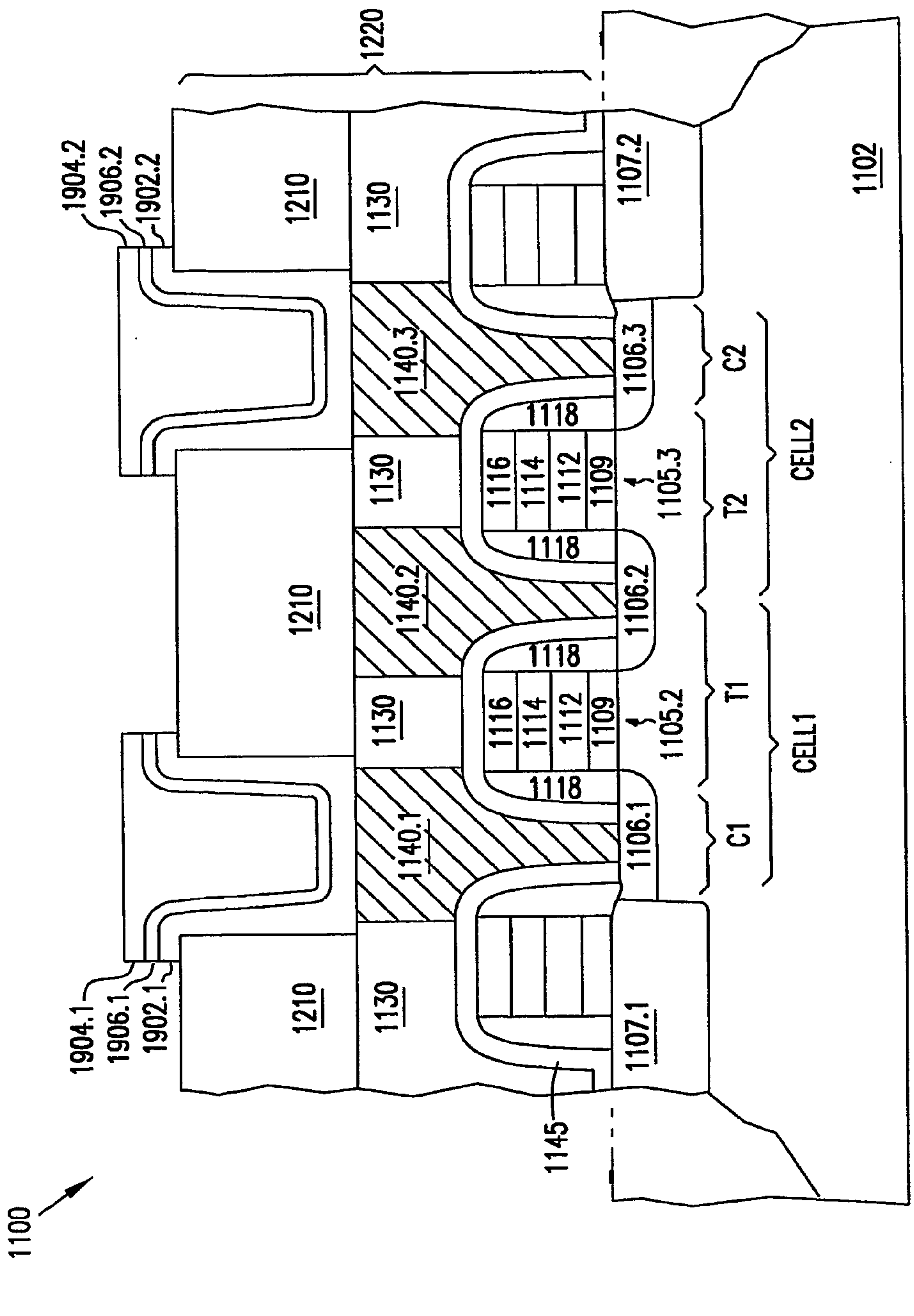

1100
1220
1904.2
1906.2
1902.2
1904.1
1906.1
1902.1
1210
1130
1140.1
1140.2
1140.3
1145
1118
1116
1114
1112
1109
1105.2
1105.3
1106.1
1106.2
1106.3
1107.1
1107.2
1102
C1
T1
T2
C2
CELL1
CELL2

FIG. 19

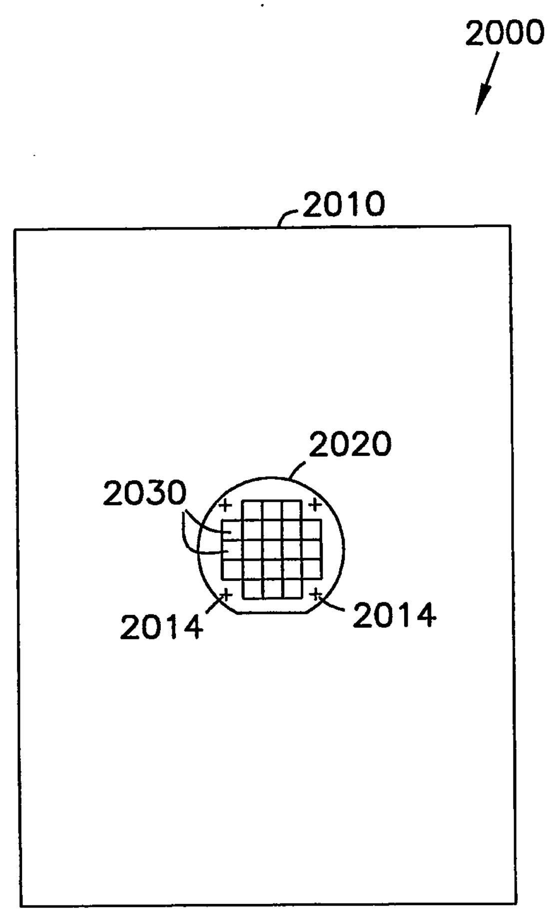


FIG. 20

INTERNATIONAL SEARCH REPORT

International Application No
PCT/US2004/029172

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L21/314

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, PAJ, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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Y	US 2002/001778 A1 (SILVETTI MARIO DAVE ET AL) 3 January 2002 (2002-01-03) paragraph '0029! - paragraph '0053!; figures 2a-2e	1-20, 32-85, 92-101
Y	US 2001/006837 A1 (KWON SE-HAN ET AL) 5 July 2001 (2001-07-05) abstract; figure 2b	21-31, 86-91, 102-112

-/--

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
24 November 2004	21/12/2004

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Bakker, J

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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

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